Announcements

- Homework #1 will be posted by 9pm tonight
  - Due Wed, Oct 8, 2pm (in class or 56-127CC)

- Your classwiki accounts (216a group) have been activated
  - 30 students have signed up so far (~20 missing)
  - Please spread the word around (for those who didn’t come to class &
    didn’t put their e-mail on the class mailing list on EEweb)
  - MSOL: check your e-mail for important announcements
    (EE account, classwiki, discussions, office hours)

- Today’s lecture
  - Technology scaling
  - MOS transistor modeling
Technology Scaling is Power Driven

1970 1985 2000
- Bipolar → NMOS → CMOS → ???
  power wall  power wall  power wall

- System performance has benefited from higher integration
- In the mid 80’s, CMOS displaced NMOS technologies to address power dissipation
  - CMOS delivered better cost performance since it was more energy efficient and improved the integration level
  - At that time CMOS was on the horizon
- Replacing CMOS by another more energy efficient technology is a distant prospect now
  - Low-power high-speed CMOS technology is becoming an indispensable, rather than desirable, technology
  - Power is the main challenge we need to address

The Limits

Theoretical Practical

- System
- Circuit
- Device
- Material
- Fundamental

Theoretical limits: physics
Practical limits: + manufacturing cost

[J. Meindl, Proc. IEEE, 1995]
Circuit Limits

- #1: logic levels (gain)
- #2: energy/transition
- #3: delay
- #4: global interconnect

Circuit Limit #1: Logic Levels (Gain)

- Distinguish logic 0's from 1's (restore logic levels → |gain| > 1)

\[ V_{dd} \geq (2kT/q)[1 + c_{fs}/(c_0 + c_d)]ln(2 + c_0/c_d) \]
\[ \geq \beta kT/q \approx 0.1V, \; (T = 300K) \quad 2 < \beta < 4 \]

[J. Meindl, Proc. IEEE, 1995]
Circuit Limits (Cont.)

- **#2: energy/transition**
  - Neglecting static current
  \[ E_{\text{tran}} = \frac{1}{2} C_L V_{dd}^2 \]

- **#3: delay**
  - Limited by
  \[ I_{\text{sat}} \approx WC_{\text{ox}} v_{\text{sat}} (V_{GS} - V_T) \]
  \[ t_d = \frac{1}{2} C_L V_{dd} \]

- **#4: global interconnect**
  - Interconnect delay should not exceed gate delay
  \[ \tau \approx (2.3 R_{\text{gate}} + R_{\text{wire}}) C_{\text{wire}} \]
  \[ R_{\text{wire}} < 2.3 R_{\text{gate}} \]

Practical Limits

- Scaling towards fundamental limits

~130nm is the most cost-effective technology (the last generation for which deep UV microlithography will suffice)

[J. Meindl, Proc. IEEE, 1995]
Practical Limits (Cont.)

- Metric: chip size \[ D = \sqrt{\text{chip area}} \]

![Graph showing chip size vs calendar year](image1)

**D = 50mm (16” wafer)**
**D = 40mm (12” wafer)**
**D = 25mm (8” wafer)**

[J. Meindl, Proc. IEEE, 1995]

---

Practical Limits (Cont.)

- Packing efficiency = # transistors / min feature area

![Graph showing packing efficiency vs calendar year](image2)

**↑ # mask levels**
**3D / vertical integration**

**↑ Layout density**

*Fig. 28. Packing efficiency \( PE \) versus calendar year \( Y \). Note that packing efficiency is defined as the number of transistors per minimum feature area.*

[J. Meindl, Proc. IEEE, 1995]
Basic Scaling Trends

- **Const \( V_{DD} \)**
- **Const \( E \)**
- **General**

Doubles every 2 years


Frequency (Mhz): 8085, 8086, 286, 386, 486

Source: S. Borkar (Intel)

Constant Electric Field Scaling

- Dimensions and voltages scale by the same factor (speed!)
  - Idea of scaling voltage OK up to the point of leakage (exp\(^{-V_{TH}}\))

[B. Davari et al., Proc. IEEE, 1995]
Scaling Overview (Fixed V, Fixed E, General)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$W, L, t_{ox}$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$V_{DD}, V_T$</td>
<td>$1$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/U$</td>
</tr>
<tr>
<td>Area/Device</td>
<td>$WL$</td>
<td>$1/S^2$</td>
<td>$1/S^2$</td>
<td>$1/S^2$</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>$1/t_{ox}$</td>
<td>$S$</td>
<td>$S$</td>
<td>$S$</td>
</tr>
<tr>
<td>$C_{gate}$</td>
<td>$C_{ox} WL$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$k_n, k_p$</td>
<td>$C_{ox} WL$</td>
<td>$S$</td>
<td>$S$</td>
<td>$S$</td>
</tr>
<tr>
<td>$I_{sat}$</td>
<td>$C_{ox} WV$</td>
<td>$1$</td>
<td>$1/S$</td>
<td>$1/U$</td>
</tr>
<tr>
<td>Current Density</td>
<td>$I_{sat}/Area$</td>
<td>$S^2$</td>
<td>$S$</td>
<td>$S^2/U$</td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>$V/I_{sat}$</td>
<td>$1$</td>
<td>$1$</td>
<td>$1$</td>
</tr>
<tr>
<td>Intr. Delay</td>
<td>$R_{on} C_{gate}$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>Power</td>
<td>$I_{sat} V$</td>
<td>$1$</td>
<td>$1/S^2$</td>
<td>$1/U^2$</td>
</tr>
<tr>
<td>P Density</td>
<td>Power/Area</td>
<td>$S^2$</td>
<td>$1$</td>
<td>$S^2/U^2$</td>
</tr>
</tbody>
</table>

High-Performance and Low-Power Flavors

[Source: T. Kuroda] [B. Davari et al., Proc. IEEE, 1995]
Reaching the Power Density Limit

- HS: out of the game
- Issues with LP
  - Soft-errors getting worse with low $V_{DD}$ and reduced cap
  - Lower limit on $V_{TH}$ (leakage)
  - Multi $V_{TH}$, multi $V_{DD}$ running out of gas

$\mu m^2$, $\mu m$ in $\mu m$

[Note: Figure with graph showing relative power density versus channel length ($L$, $\mu m$).]

MOS Transistor Modeling

- Many levels
  - Hand analysis
  - CAD analysis (e.g. Matlab)
  - Switch-level analysis (e.g. PrimeTime)
  - Circuit simulation (e.g. Spectre, HSPICE)

- These levels have different requirements in complexity, accuracy, and speed of convergence

- We are primarily interested in delay and energy modeling, rather than current modeling (but have to start from the currents)…
MOSFET, Notations

- Lateral diffusion
- Lower potential n+ sources e⁻ to current flows to higher potential n+ (drains e⁻)

General I-V Characteristic (Qualitative View)

- Fixed VGS, increasing VDS: general I-V shape
  - Ip: non-saturation
  - Ip: saturation (large VGS)
  - Ip: saturation (small VGS) above Vt

- In saturation, VDS drains all e⁻ that can be supplied by the channel
- Transition b/w linear and sat is smooth, but sometimes taken to be at a specific point, for convenience
- BODY BIAS: VGS > 0 ⇒ population of channel e⁻ ↑ ⇒ Ip ↓
Deep Submicron MOS I-V Model

- **Define** $V_{GT} = V_{GS} - V_T$

  - **For** $V_{GT} \leq 0$ (sub-$V_{TH}$):
    \[
    I_{DS} = I_0 \cdot \frac{W}{L} \cdot \frac{V_{GS} - V_T + V_{DS}}{s} \cdot (1 + \lambda \cdot V_{DS})
    \]

  - **For** $V_{GT} \geq 0$ (Lin, Sat, V-Sat):
    \[
    I_D = k' \cdot \frac{W}{L} \cdot \left( V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})
    
    \text{with } V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})
    \]

Important Concepts to Understand

- Threshold voltage (review EE115C / lecture 2)
- Channel length modulation (channel pinch-off)
- Velocity saturation

**CLM** one of the first “short-channel” effects (also noticeable for sub-micron channels)
Modeling Channel Length Modulation (CLM)

- Many empirical models
  - Goal: get a simple model that is convenient for hand analysis
  - Here is a possible modeling approach:

\[
I_{DS} = \frac{\text{const}}{L_{eff} - L_p} = \frac{I_{ph}}{L_{eff} - L_p} \approx I_{P3} \left( 1 + \frac{L_p}{L_{eff}} \right)
\]

\[
l_d = f(V_{DS}) \sim \sqrt{V_{DS}} \quad \text{or} \quad h_n(V_{DS}) \quad \text{(several models)}
\]

CLM Model

Simple empirical models:
\[\begin{align*}
a) \quad I_{DS} &= I_{DS0} \left( 1 + \frac{V_{DS} - V_{MOS}}{V_{TH}} \right) \\
b) \quad I_{DS} &= I_{DS0} \left( 1 + \frac{V_{DS} - V_{MOS}}{V_{TH} + V_{BS}} \right)
\end{align*}\]

Empirical model:
\[\left( 1 + \gamma V_{BS} \right)\]  
Typical values 0.05-0.5  
\(V_{BS}\) dependent
**Important Concepts to Understand**

- Threshold voltage
- Channel length modulation (channel pinch-off)
- Velocity saturation

**VELOCITY SATURATION**

\[ v_n = \frac{\mu n \cdot \xi}{1 + \xi / \xi_c} \quad \text{for} \quad \xi \leq \xi_c \]

\[ v_n = v_{sat} \quad \text{for} \quad \xi > \xi_c \]

(continuity)

\[ v_{sat} = \frac{\mu n \cdot \xi}{2} \]

**Including Velocity Saturation**

- Approximate velocity:

  \[ v_n = \frac{\mu n \cdot \xi}{1 + \xi / \xi_c} \quad \text{for} \quad \xi \leq \xi_c \]

  \[ v_n = v_{sat} \quad \text{for} \quad \xi > \xi_c \]

**A more general model:**

\[ v_n = \frac{\mu n \cdot \xi}{(1 + (\xi / \xi_c)^n)^{1/n}} \]

we use \( n = 1 \)

- And integrate current again:

\[ I_D = \frac{\mu n \cdot C_o x}{1 + V_{DS} / \xi_c L} \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right] \]

In **deep submicron**, there are four regions of operation:

1. cutoff
2. resistive
3. saturation
4. **velocity saturation**
Including Velocity Sat. in the $I_D$ Formula

Modified $I_D$ formula:

$$I_D = \frac{K_{m} \cdot W}{L} \left[ (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] = I_{DSAT} @ V_{DSAT}$$

$$I_{DSAT} = W \cdot \mu \cdot \frac{2}{2} \left[ (V_{GS} - V_{TH} - V_{DSAT}) \right]$$

$$\frac{M_{w} \cdot C_{ox} \cdot W}{2} \left( \frac{V_{GT} - V_{DSAT}}{2} \right) = \frac{M_{w} \cdot C_{ox} \cdot W}{1} \left( \frac{V_{GT} \cdot V_{DSAT} - V_{DSAT}^2}{2} \right)$$

$$\left( \frac{\varepsilon_{cL} \cdot V_{GT} + V_{DSAT}}{2} \right) \left( \frac{V_{GT} - V_{DSAT}}{2} \right) = V_{GT} \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}$$

$$\frac{\varepsilon_{cL} \cdot V_{GT} - \frac{\varepsilon_{cL} \cdot V_{DSAT} - V_{GT} \cdot V_{DSAT}}{2}}{2} = 0$$

$$V_{DSAT} = V_{GT} - \frac{V_{GT} \cdot V_{DSAT} - V_{DSAT}^2}{1 + \frac{V_{GT} \cdot V_{DSAT}}{2}} = K \cdot V_{GT}$$

Saturation vs. Velocity Saturation

- V-Sat occurs for lower $V_{DS}$ than Sat

Diagram showing the relationship between $I_D$, $V_{DS}$, $V_{GS}$, and $V_{TH}$. The CLM also holds in $V_{SAT}$.
Another Look at Velocity Saturation

- Long-channel device
  - $V_{GS} = V_{DD}$
  - $V_{DS} = V_{DSAT}$
  - $V_{GS} - V_T$

- Short-channel device
  - $V_{DS} > V_{GS} - V_T > 0$

$I_D$ versus $V_{GS}$ (Assume $V_{DS} > V_{GS} - V_T > 0$)

- Long Channel (always Sat)
- Quadratic (Sat)
- Linear (V-Sat)
- Short Channel (Sat or V-Sat)
- Quadratic (Sat)

- small $V_{GS}$
- large $V_{GS}$
Simple Model vs. SPICE Simulation

- Transition between lin/v-sat has the largest modeling error

![Graph showing comparison between simple model and SPICE simulation](image)

Long vs. Short Channel (Simulation Data)

- 90nm device, constant W/L ratio
  - Long Channel: W/L = 2.4µm/0.5µm
  - Short Channel: W/L = 480nm/100nm

![Graph showing long vs. short channel comparison](image)

- Observations
  - Short L (100nm) has larger impact of CLM on \( I_D \)
  - Linear separation of V-Sat curves (red), quadratic for Sat (blue)
  - \( I_D(V\text{-Sat}) < I_D(Sat) \) at large \( V_{GS} \)
MOS Regions of Operation

- Nano-scale MOS devices operate in velocity saturation
  - Saturation still possible for low $V_{GS}$ values (up to $V_{DSAT}$)

Unified Formula for the Drain Current

- Many modes of operation can be nicely captured with a single formula:

\[
I_D = \frac{W}{L} \times \frac{C_\text{ox}}{2} \times \left( V_{GS} - \frac{V_{TH}}{2} \right) \times (1 + \lambda \times V_{DS})
\]

It introduces CLM into linear region, but this works fine because of small $V_{DS}$ in linear mode.

Left = 70 nm

$\varepsilon = 4 \text{ V/\text{um}} \implies V_{DSAT} = \varepsilon \cdot \text{Left} = 0.3 \text{V}$
Unified Model: Observations

- CLM term \(1 + \lambda V_{DS}\) also included for linear region
  - Empirical, not grounded in physical considerations

- Five parameters: \(V_{T0}, \gamma, V_{DSAT}, k', \lambda\)
  - Can determine from physics
  - Or choose values that best match simulation data
    (match the best in regions that matter the most)
  - Use different model for \(L >> L_{min}\)
    (we assume \(L = L_{min}\) unless otherwise specified)

Let's see how to extract these key parameters from the I-V curves

The Meaning of Model Parameters

\[
\begin{align*}
V_{T0} & = \frac{I_{D1}}{I_{D2}} = \frac{(V_{GSS} - V_{T0})^2}{(V_{GSS} - V_{T0})^2} = V_{T0} \\
\gamma & = \text{same as for } V_{T0} \rightarrow \text{estimate } V_T \\
V_T & = V_{T0} + \gamma (\sqrt{2\phi_f + \gamma_{SB}} - \sqrt{2\phi_f}) \rightarrow \text{calculate } \gamma \\
\lambda & = \frac{1 + \lambda V_{DS}^1}{1 + \lambda V_{DS}^2} = \frac{I_{D1}}{I_{D2}} \Rightarrow \lambda \\
\lambda & = \text{assume } \lambda \text{ known from previous calculations} \\
I_D & = \lambda \frac{I_{D1}}{V_{GSS}} (V_{GSS} - V_{T0})^2 (1 + \lambda V_{DS}^2) \Rightarrow \lambda
\end{align*}
\]
Alpha Power Law Model

- Alternate approach, useful for hand analysis
  - Works better for delay than current

\[ I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L}(V_{GS} - V_{T})^\alpha \]

- Empirical model
  - Curve fitting (MMSE)
  - \( \alpha \) is between 1 and 2
  - In 90nm, it is about 1.4
    (note: it depends on \( V_{T} \))
      - Can fit to \( \alpha = 1 \), but with what \( V_{T} \)?

[ T. Sakurai, R. Newton, JSSC, Apr. 1990 ]

Second Order Effects

- Drain Induced Barrier Lowering (DIBL)
- Reverse Short Channel Effect (RSCE)
- Narrow Width Effects (NWE)
- Hot Carriers (HC)
Drain Induced Barrier Lowering (DIBL)

\[ \Delta V_T \approx -2\beta L \frac{V_S}{2} \left[ \left( V_{GS} + V_{BB} \right) + \beta \Delta V_S \right] \]

\( \Rightarrow \) even if we neglect CDM, \( I_{DS} \) will increase with \( V_S \) if \( \Delta V_T \)
\( \Rightarrow \) device turned off by \( V_S \), below \( \Delta V_T \) may turn on by \( \Delta V_S \)

Threshold Variations

Long-channel threshold

\[ \text{Threshold as a function of channel length (for low } V_{DS} \text{)} \]

Low \( V_{DS} \) threshold

Drain induced barrier lowering (DIBL) (for low \( L \))

\[ I_{DS, SC} = I_{DS, LC} \cdot e^{-\frac{\Delta V_T}{V_T}} \]

These factors in \( I_{DS, SC} \) V/VOS in sub-threshold formula
DIBL and RSCE

- RSCE is typical in today’s processes
  - Tradeoff between leakage power and performance

The Hot Carrier (HC) Effect

- Gets worse with technology scaling (shorter L)

\[
\begin{align*}
E & > E_c \text{ for HC} \\
\text{energy of } e^- & \text{ to jump into oxide} \\
\text{occurs } v=\text{sat} \\
\text{carriers acquire kinetic energy from the field, but their} & \\
\text{velocity is randomized by excessive collisions such that} & \\
\text{their velocity along the field direction no longer} & \\
\text{increases but their random kinetic energy does} \\
\end{align*}
\]
**HC Effect Shows up Over Time**

- Current drops over time due to HC

![Graph showing current drops over time due to HC](image)

- $I_d$ due to HC effect (exhibited over time)
- $V_T \uparrow$ for NMOS
- $V_T \downarrow$ for PMOS

**Sub-threshold Current**

- This is another topic of crucial importance in digital design
  - We need to consider sub-threshold current, because digital designs have many millions of transistors and when these are inactive, we may get some lots wasted power...

$$I_d \text{ does not drop abruptly to } 0 \text{ if } V_{GS} = V_T$$

- Transition from "on" to "off" is gradual
- Parasitic BJT model makes sense for short $L$
Sub-threshold $I_D$ versus $V_{GS}$ is Exponential

Modeling the Sub-threshold Behavior

$$V_{BE} = V_{DD} = \frac{V_{GS}}{1 + \frac{C_d}{C_{ox}}}$$

BJT: $I_C = I_0 e^{V_{GS}/b_0}$

Formula for $I_0$:

$$I_0 = \frac{W}{L} \left( \frac{kT}{2} \right) e^{-\frac{V_T}{kT}}$$

Another formula:

$$I_0 = \frac{W}{W_0} 10 \frac{V_{GS} - V_T + 2V_{th}}{3} (1 + 2V_{th})$$
The Sub-threshold Slope Parameter

- Meaning: change in $V_{GS}$ that gives 10x change in $I_{DS}$

$$S = n \left( \frac{kT}{I} \right) \ln 10 \frac{mV}{\text{dec}}$$

- $S$ increases with temperature.
- $n$ is intrinsic device topology and structure.
- Different process technology e.g., SOI.

Sub-Threshold $I_D$ vs. $V_{GS}$

**Physical model**

$$I_{DS} = I_0 \cdot e^{- \frac{V_{GS}}{S}} \cdot (1 - e^{- \frac{V_{DS}}{kT/q}}) \cdot (1 + \lambda \cdot V_{DS})$$

$$I_0 = \mu \frac{W}{L} \frac{kT}{q} e^{- \frac{V_T}{q}}$$

**Empirical model**

$$I_{DS} = \frac{I_0 \cdot W}{W_0} \cdot 10^{\frac{V_{GS} - V_T + V_{DS}}{S}} \cdot (1 + \lambda \cdot V_{DS})$$

$$S = n \frac{kT}{q} \ln(10) \quad [mV/\text{dec}]$$
Example (90nm): Sub-Threshold $I_D$ vs. $V_{GS}$

$$I_{DS} = I_0 \frac{W}{W_0} 10^{\frac{V_{GS}-V_T+V_{DS}}{S}} (1 + \lambda V_{DS})$$

$$S = \frac{kT}{q} \ln(10)$$

$90mV/\text{dec}$

$V_{DS}$ from 0 to 0.4V

---

Example (90nm): Sub-Threshold $I_D$ vs. $V_{DS}$

$$I_{DS} = I_0 \frac{W}{W_0} 10^{\frac{V_{GS}-V_T+V_{DS}}{S}} (1 + \lambda V_{DS})$$

$$S = \frac{kT}{q} \ln(10)$$

$gpd090$

$V_{GS}$ from 0 to 0.3V
Stack Effect

- Transistor stacks greatly reduce leakage

NAND gate

Leakage power reduction


Deep Submicron MOS I-V Model (Summary)

Define \( V_{GT} = V_{GS} - V_{T} \)

For \( V_{GT} \leq 0 \) (sub-\( V_{TH} \)):

\[
I_{DS} = I_0 \cdot \frac{W}{W_n} \cdot 10^{\frac{V_{GS} - V_{T} + V_{DS}}{\lambda S}} \cdot (1 + \lambda \cdot V_{DS})
\]

For \( V_{GT} \geq 0 \) (Lin, Sat, V-Sat):

\[
I_D = k' \cdot \frac{W}{L} \cdot \left( V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})
\]

With \( V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}) \)

Sat Lin V-Sat
Non-Ideal Behavior: Summary

- MOS transistor has 4 terminals (the fourth being the substrate/body)
  - Although it does not conduct significant current, it can impact performance.
  - Body effect: impacts how easy/difficult it is to turn on \( V_T \) the gate.

- The current in Saturation is not independent of \( V_{DS} \)
  - Especially as length is being scaled down with each generation.
  - Channel length modulation: the effective channel length is actually a function of the \( V_{DS} \).
  - Drain-induced barrier lowering
    * High \( E_{DS} \) must have an effect. \( V_T \) reduces as drain voltage increase.

- Velocity saturation
  - Charge velocity reaches a maximum with high \( E_{DS} \) (occurs primarily with device in Saturation)

- Subthreshold current
  - Small amount of current still trickles when \( V_{GS} < V_T \)

Actual gpdk090 Model (gpdk090_mos.scs)

section TT_s1v
parameters
+ s1v_rs_ne = 0.000000e+000  s1v_vsat_ne = 1.120000e+005  s1v_pldd_surf =
+ s1v_u0_ne = 3.700000e+010  s1v_u0_ne = 2.000000e-002  s1v_nch_ne = 5.200000e+017
+ s1v_rsc_ne = 4.082483e-014  s1v_bgbo_ne = 1.482000e+011  s1v_pldtn_ne = 1.000000e+001
+ s1v_rdc_ne = 4.082483e-014  s1v_vto0_ne = 1.692662e-001  s1v_s2_ne = 0.000000e+000
+ s1v_cog0_ne = 2.667600e-010  s1v_cgs0_ne = 4.865336e+000  s1v_wmne = 6.000000e+009
+ s1v_k1_ne = 2.825346e-001  s1v_cgs1_ne = 1.111500e+010  s1v_nidd_surf =
+ s1v_js_ne = 3.368667e-006  s1v_hdf_ne = 1.400000e+007  s1v_rds0_ne = 3.900000e-006
+ s1v_cjw_ne = 3.366667e+010  s1v_box_ne = 2.330000e-009  s1v_cj_ne = 7.983537e-004
+ s1v_cjw_ne = 4.790122e+011  s1v_xj_ne = 7.983537e-004  s1v_rsc_ne = 2.500000e+000
+ s1v_vio_ne = 0.000000e+000  s1v_pb_ne = 9.198524e-001  s1v_cj_ne = 4.594812e-011
+ s1v_vio_ne = 1.500000e-008  s1v_vjw0_ne = 1.995884e-011  s1v_rsh_ne = 1.000000e+001
+ s1v_vio_ne = 1.200000e+002  s1v_rch_ne = 4.000000e+017  s1v_rsc_ne = 2.868515e+014
+ s1v_cog0_ne = 1.392363e-011  s1v_vrd0_ne = 2.868515e+014  s1v_vjw0_ne = -1.359511e+000
+ s1v_vio_ne = 0.000000e+000  s1v_vjw0_ne = 2.506253e-010  s1v_cjw0_ne =
  1.043477e+001
+ s1v_vio_ne = 5.000000e-009  s1v_k1_ne = 2.637520e-001  s1v_cjw_ne = 1.044272e+010
+ s1v_vio_ne = 3.350000e-006  s1v_hdf_ne = 1.400000e+007  s1v_vds0_ne = 7.800000e-009
+ s1v_vio_ne = 3.350000e+010  s1v_tox_ne = 2.480000e-009  s1v_cj_ne = 7.912252e+004
+ s1v_vio_ne = 4.747351e+011  s1v_ldf_ne = 1.000000e-008  s1v_vj_ne = 2.500000e+008
+ s1v_vio_ne = 1.500000e+008  s1v_vjw0_ne = 1.000000e+009  s1v_cj_ne = 4.527119e+011
+ s1v_vio_ne = 1.000000e+000  s1v_vjw0_ne = 2.000000e+001

include "gpdk090_mos.scs" section
endsection TT_s1v
And many more parameters... (compare to our 5-parameter model)