ENT  ENTITY rtl_counter IS  
PORT(clk: IN BIT; 
    Z: OUT BIT); 
END rtl_counter; 

ARCHITECTURE general OF rtl_counter IS  
TYPE stateT IS (S0, S1); 
SIGNAL state : stateT := S0; -- state register 
SIGNAL reg_A : BIT; -- data register 
SIGNAL data_ctrls : BIT; -- controls 
SIGNAL data_conds : BIT; -- conditions 
BEGIN 
  --datapath subsystem 
  PROCESS(clk) 
  VARIABLE w : BIT; 
  BEGIN 
    CASE data_ctrls IS 
      WHEN '1' =>  w:= '1'; 
      WHEN '0' =>  w:= '0'; 
    END CASE; 
    IF (clk’EVENT AND clk = ‘1’) THEN 
      reg_A <= w; 
    END IF; 
  END PROCESS; 
  --controller subsystem 
  --state transition function 
  PROCESS (clk) 
  BEGIN 
    IF (clk’EVENT AND clk = ‘1’) THEN 
      CASE state IS 
        WHEN S0 => IF (data_conds = ‘0’) THEN state <= S1; 
        ELSE state <= S0; END IF; 
        WHEN S1 => IF (data_conds = ‘1’) THEN state <= S0; 
        ELSE state <= S1; END IF; 
      END CASE; 
    END IF; 
  END PROCESS; 
  --controller output function 
  PROCESS(state) 
  BEGIN 
    CASE state IS 
      WHEN S0 => data_ctrls <= ‘0’; 
      WHEN S1 => data_ctrls <= ‘1’; 
    END CASE; 
  END PROCESS; 
END general;
Reg A

Controller

data_conds

S0/0

0

1

S1/1

0

1

data_ctrls

Z

Datapath

Req A

w

0

1

clk