Introduction

- EEM16: Logic Design of Digital Systems (section 1)
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Course Webpage

- http://www.eeweb.ee.ucla.edu
- Assignment and handouts are uploaded
Topics

- Introduction to VHDL
- Two mini projects using VHDL
- Topics that the class does not cover
  - Tabular logic minimization method
  - State minimization
- Midterm reviews
- Q&A
Hardware Description Language

- Standard language for documentation and automation of design process (simulation, synthesis, description of implementation) in computer systems
Design Process of Digital Systems

Specification → Implementation → Verification

Correct? Yes → Fabrication

Correct? No → Library → Specification
VHDL and Verilog

- VHDL (VHSIC: Very High Speed Integrated Circuit Hardware Description Language)
  - USA Department of Defense initiated VHDL for self documenting of circuit design in 1980 and IEEE ratified the language as IEEE Standard 1076.

- Verilog
  - Verilog was born from CAE software companies.
library IEEE;
use IEEE.std_logic_1164.all;

-- entity
ENTITY And4 IS PORT (  
a, b, c, d: IN std_logic;  
z : OUT std_logic);
END And4;

-- architecture
ARCHITECTURE behavioral OF And4 IS
BEGIN
  PROCESS(a,b,c,d)
  BEGIN
    IF (a='1' and b='1' and c='1' and d='1') THEN z <= '1';
    ELSE z <= '0';
    END IF;
  END PROCESS;
END behavioral;
VHDL Module

- Consists of Entity and Architecture
- Entity describes interface (input and output) of the module
- Architecture describes its functionality

NOTE: VHDL does not distinguish lowercase and uppercase letters.
ENTITY Body

- Signal Mode : Signal Type
- Signal Mode
  - IN
  - OUT
  - BUFFER
  - INOUT

ENTITY adder IS
  PORT(x,y : IN BIT;
       z   : OUT BIT);
END adder;
ARCHITECTURE Body

- Behavioral vs. Structural
  - Behavioral architecture
    - describes the behavior of the module
  - Structural architecture
    - describes connections between sub-modules
Behavioral Architecture Body

- Behavioral description of an adder

```
ARCHITECTURE behavioral OF adder IS
BEGIN
  PROCESS(x, y)
  BEGIN
    z <= x + y;
  END PROCESS;
END behavioral;
```
Behavioral Architecture Body

Behavioral description of an adder

ARCHITECTURE behavioral OF adder IS
BEGIN
  PROCESS (x, y)
  BEGIN
    z <= x xor y;
  END PROCESS
END behavioral;
Behavioral Architecture Body

- Behavioral description of an adder

ARCHITECTURE behavioral OF adder IS
BEGIN
  PROCESS(x, y)
  BEGIN
    IF (x='0' and y='0') THEN z <= '0';
    ELSIF (x='1' and y='0') THEN z <= '1';
    ELSIF (x='0' and y='1') THEN z <= '1';
    ELSIF (x='1' and y='1') THEN z <= '0';
  END PROCESS
END behavioral;
Structural Architecture Body

- Interconnection between sub-modules

ARCHITECTURE structural OF adder IS
  SIGNAL s1: BIT;
BEGIN
  U1: XOR_GATE PORT MAP (A=>x, B=>y, Y=>s1);
  U2: BUF_GATE PORT MAP (A=>s1, Y=>z);
END structural;

\[ \text{Diagram showing connections between gates U1 and U2 with inputs X, Y, s1, and output Z.} \]
Materials about VHDL

- Textbook
  - Combinational circuits: Chapter 2, 3 and 4
  - Sequential circuits: Chapter 7 and 8

- Online
  - http://www.cs.ucla.edu/Logic_Design/vhdlinintro.html
  - Google “Introduction to VHDL”
MAX-PLUS II

Installation

- Insert the CD at the back of the textbook into PC
- Goto CD/PC/MAXPLUS2
- Run install.exe
- Get authorization code from http://www.altera.com/support/licensing/lic-index.html (at the bottom of this page)
- Fill the information and request authorization code
- Invoke MAX-plus II and enter the authorization code