Design of VLSI Circuits and Systems (M216A)
Prof. C.K. Ken Yang
Fall 2004-2005

Course Information
Description: This course will cover the entire process of designing a digital VLSI system. We will begin with a review of how MOS transistors operate and how to use transistors in building logic gates. These topics will be taught with using them as building blocks of a larger system in mind. After the review, our focus will shift to top-down design by learning a hardware description language (Verilog-HDL). The remainder of the course covers how this programming language maps into the digital circuits. We will synthesize gate-level implementation from the hardware description. Following which, we will place the gates in a physical implementation. The timing of the circuit will be verified as the final step. Synopsys, and Cadence tools will be used in this design process. In addition, we will discuss system-level issues such as datapath/control partitioning, floorplanning, clocking strategies, and gate sizing.
Prerequisite: Logic design course (CS-51), basic transistor theory (EE115A), and recommended EE-115C or equivalent
Location: MW 2:00-3:50, Knudsen 1240B
Textbook: N. Weste, D. Harris, CMOS VLSI Design, Addison Wesley
J.M. Rabaey, Digital Integrated Circuits, Prentice Hall (Highly recommended)
Other references are tutorials and handouts that will be available on-line.

Teaching Staff Information
Instructor: C.K. Ken Yang (yang@ee.ucla.edu)
Office: 56-147A Phone: (310) 206-3665
Instructor OH: W: 1600-1700, T: 1000-1100 (56-147A)
Lab Assistant: Jaeseo Lee (ee216a@ee.ucla.edu)
Lab Sessions: MW:900-1100, T:1600-1800(HP Lab 5th floor Engr IV) (First hour is normal office hours on days without labs.)
Web-site: http://www.eeweb.ee.ucla.edu
Note that you need to apply for a seasnet account (www.seas.ucla.edu/acctapp/)
You should also have an EE-net account. Please apply for one if you are an EE student. If you are not an EE student, I will provide one.
Administrator: Christian McKenly 66-127CC EIV

Grading
Exams: Midterm (25%), Final Exam (40%) on Dec. 15 (1130 - 1430)
Homeworks: Homeworks+Mini-project (35%)
Late Policy: All homeworks are turned in during class. No late homework. In cases of extenuating circumstances, the instructor must be informed 1 day in advance.
Regrade Policy: Complaints regarding any grading are directed to the instructor. Complaints are to be written on a cover sheet. The entire exam/homework will be regraded.