1. Draw the function for 
\[ F = A(B+C) \]
using switch logic. Use A as the switch inputs and assume that switches with complemented gate inputs are available.

2. Calculate the average diffusion capacitance, \( C_{db} \), of the drain of a contacted NMOS transistor with \( W=1.2\mu m \) \((4\lambda)\), in \( 0.6-\mu m \) \((\lambda=0.3\mu m)\) CMOS technology. The contact causes the length of the drain to be \( 5\lambda \). Assume that the drain voltage linearly sweeps between 0V and 5V. Assume that \( C_{J0}=0.42fF/\mu m^2, M_J=0.44, C_{JSW0}=0.33fF/\mu m, M_{JSW}=0.12, \) and \( V_o=0.98V \). Note that the JSW parameters refer to the side wall (perimeter not including the side with the channel).

3. For parts (a) and (b), determine the appropriate final value for \( V_o \) (assuming that it is a capacitive load and no body effect) for each of the two networks shown below. Let \( V_{DD}=2.5V \). Assume all floating nodes to be initialized to \( V_{DD} \). Also assume no leakage in this case.
   For part (c) assume that there is body effect where \( \phi_s=0.8V \) and \( \gamma=0.3V^{1/2} \), calculate the \( V_o \) for the (b) network.

4. For a 10-\( \mu m \) NMOS transistor with its source grounded, let \( V_{T0}=0.5V \) (at 25°C), the saturation current (at 25°C) is \( I_{dssat}=0.6mA/\mu m, k_{VT}=1mV/K, k_\mu=-1.5, \) leakage current (at 25°C) is 50nA/\( \mu m \), and \( n=1.4 \). Assume that \( V_{DD} \) can vary by +/-10% and temperature can change between 25°C to 125°C.
   (a) What Supply and Temperature conditions would give the worst drive current (for speed)? Justify your answer.
   (b) What Supply and Temperature conditions would give the worst subthreshold leakage (for power)? Justify your answer.

5. Compare the effective pull-up saturation current of a single 1-\( \mu m \) PMOS transistor with a series connected (3-stack) PMOS transistors each 1\( \mu m \). Ignore body effect. Use the alpha-power model for the PMOS where \( V_{thp}=-0.5, \alpha=1.5, \beta=220\mu A/V^2 \) \((W=1\mu m)\), \( P_c=0.72, P_v=0.6, \) and \( V_{DD} (V_{SG})=2.5V \).
6. You are to design the following function. Assume $\lambda = 0.12\mu$m for the technology.

$$X = \overline{A} + (\overline{B\overline{C}})(\overline{D} + \overline{E})$$

(a) Design a single Static CMOS gate that performs the function.
(b) Given that $\mu_p$ and $\mu_n$ are 220cm$^2$/V-s, 550cm$^2$/V-s respectively, find the sizes (in lambdas) for the devices if the worst-case pull-down strength of the gate is equivalent to that of a CMOS Inverter with an NMOS size of 4 lambdas, and the worst-case pull-up has the same strength. Ignore velocity saturation.
(c) Repeat part (b) by including the impact of velocity saturation. Use the simplification from the notes where $R_{nostack_pdn} = (4/3)R_{stack_pdn}$ and $R_{nostack_pup} = (6/5)R_{stack_pup}$.
(d) Estimate the worst case delay for both rising and fall of the gate design in (c) if the gate drives a load of 10fF. Use the following for resistances (stacked) and capacitances. $C_{S/D} = 1.5\text{fF}/\mu\text{m}$, $C_G = 2\text{fF}/\mu\text{m}$, $R_P = 7.5\text{k}\Omega - \mu\text{m}$, $R_N = 3\text{k}\Omega - \mu\text{m}$. Be sure to use Elmore Delay. Be sure to account for velocity saturation as in part (c).