9.1

a. 
\[ z_0 = x'_4 x'_3 x'_2 x'_1 x_0 \]
\[ z_1 = x_4 x_3 x'_2 x'_1 x'_0 \]
\[ z_2 = x_4 x'_3 x'_2 x'_1 x'_0 \]
\[ z_3 = x'_4 x_3 x_2 x'_1 x'_0 \]
\[ z_4 = x_4 x_3 x'_2 x_1 x'_0 \]
\[ z_5 = x'_4 x'_3 x'_2 x'_1 x'_0 \]
\[ z_6 = x'_4 x'_3 x'_2 x_1 x'_0 \]
\[ z_7 = x_4 x'_3 x'_2 x'_1 x'_0 \]
\[ z_8 = x'_4 x'_3 x'_2 x'_1 x'_0 \]
\[ z_9 = x'_4 x'_3 x'_2 x'_1 x'_0 \]

Use NAND gates to implement each switching expression as follows.

b. 
\[ z_0 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_1 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_2 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_3 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_4 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_5 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_6 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_7 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_8 = x'_3 x'_2 x'_1 x'_0 \]
\[ z_9 = x'_3 x'_2 x'_1 x'_0 \]

Use NAND gates to implement each switching expression as follows.
c.  
\[ z_0 = x_3'x_2'x_1'x_0' \]
\[ z_1 = x_3'x_2'x_1'x_0 \]
\[ z_2 = x_3'x_2'x_1x_0' \]
\[ z_3 = x_3'x_2'x_1x_0 \]
\[ z_4 = x_3'x_2x_1'x_0' \]
\[ z_5 = x_3x_2'x_1x_0 \]
\[ z_6 = x_3x_2x_1'x_0' \]
\[ z_7 = x_3x_2x_1'x_0 \]
\[ z_8 = x_3x_2x_1x_0' \]
\[ z_9 = x_3x_2x_1x_0 \]

Use NAND gates to implement each switching expression as follows.

![NAND gate diagram]

9.17  
a.
9.22
\[ z = (w \otimes f)(d \otimes g)(e \otimes h) = ((w \otimes f) + (d \otimes g) + (e \otimes h)) \]
\[ w = b'c'0 + b'ca' + bc'1 + bca = b'ca' + bc' + bca = b'ca' + bc' + ba = b'(ca') + b(ca') = b \otimes (ca') \]