Use VHDL to implement the following gate network.

1. Separate the design of counter into datapath and controller.
2. Use behavioral VHDL to write the counter module and the multiplexer module.
3. Use structural VHDL to write the system i.e. connecting the counter and multiplexer together. Inputs of the system are clk, en, x0, x1, x2 and x3. Output of the system is z.
4. The counter should be triggered by low-to-high signals of “clk”.
5. The counter should be working when “en” is set to be high, while disabled when “en” is set to be low.
6. The multiplexer should be working when “en” is set to be high, while disabled when “en” is set to be low.

Your report should includes
1. One figure which indicates the interface between your datapath and controller of the counter.
2. One figure which indicates your counter datapath design.
3. One figure which indicates your counter controller state transition diagram.
4. Printed VHDL for counter module, multiplexer module and the system as attachments.

The report should be turned in after the lecture on June 10th.

END