In this project, each group of two will design a fully differential wide-band op-amp intended for use in a 1st-order RC low-pass filter.

**Design Specifications**

The low-pass filter shown below must satisfy the following requirements:

- Gain = 5, with less than 1% error
- 3-dB Bandwidth = 9.95MHz, with less than 1% error
- HD3 < 1% for a 2 MHz input tone, with 1.6V peak-to-peak differential output swing
- Open loop phase margin > 60° (C2 can be removed for phase margin calculations)
- Supply voltage = 1.8V

The value of C2 is set to 1.6pF based on the noise requirements. The values of R1 and R2 are set to 2kΩ and 10kΩ respectively. With an ideal op-amp, the gain of the filter is 5 with a 3-dB bandwidth of about 9.95MHz. However, due to the op-amp non-idealities, the overall gain and bandwidth of the filter will be lower than the targeted values. The goal is to design an op-amp to maintain better than 1% gain and bandwidth error, while achieving the best possible power consumption. Cp1 and Cp2 are the routing parasitics at the input and output and are each 200fF. The filter is driving an identical stage at its output.

**Simulations**

The op-amp must be designed and simulated using the TSMC 0.18µm model file which can be downloaded at: [https://www.eeweb.ee.ucla.edu/images/upload/215A_1_mm018.scs](https://www.eeweb.ee.ucla.edu/images/upload/215A_1_mm018.scs)

The minimum allowable width of drain and source regions in this process is 0.5µm. This should be used for drain and source junction capacitance calculations. All the design specifications must be simulated and well documented. It is helpful to start the design by developing first order equations to justify the design choices.

**Project Report**

Your report is an important part of your final project. It should be a concise, yet accurate representation of your design, describing the circuit details and simulation results. The entire report, including the simulation results must not exceed 10 pages.