Problem #1
For a Static CMOS gate with the following function (without sizing)
\[ f = a'(e' + (b + c + d)') \]
(a) Assuming no velocity saturation (very large \( E_C \)), size all the devices of the logic gate for roughly equal delays. Use a reference inverter with PN ratio of square-root(3), 1.7. This sizing happens to be for minimum average delay instead of equal rise-and-fall. Let \( \mu_{NCOX} = \mu_{PCOX} \). Let \( W_A \) to be the size of the NMOS device whose gate input is “a”. Size all devices relative to \( W_A \).
(b) If the NMOS device whose gate input is “a” is velocity saturated, how much bigger must an NMOS device be (relative to a non-velocity saturated device) to pull the same current (and hence have the same resistance). For this problem, assume that \( V_{DD} = 2.5V, V_{TN} = -V_{TP} = 0.5V, L_{eff} = 0.2\mu m \) (both PMOS and NMOS), and \( E_{CN} = 5V/\mu m, E_{CP} = 7V/\mu m \).
(c) Using the same assumptions for velocity saturation as in part (c), resize the devices for equal rise and fall delays. Use \( W_{AX} \) to be the size of the NMOS device whose gate input is “a”. Size everything relative to \( W_{AX} \).

Problem #2
For the logic gate shown to the right, calculate the delay of this logic gate from each input-to-output for both rising and falling output transitions. Use the RC time-constant method. You can assume that this logic gate is driving the “a” input of the same gate (with the same sizing). Assume that the output, \( f \), is driving an extrinsic load of 25fF. You can ignore velocity saturation for any series-stacking greater than 1. For this problem, assume that \( V_{DD} = 2.5V, V_{TN} = -V_{TP} = 0.5, L_{eff} = 0.2\mu m \) (both PMOS and NMOS), \( k_{CG} = 2fF/\mu m \), \( k_{CD} = 1.5fF/\mu m \), \( \mu_{NCOX} = 3\mu m^2/V^2 \) and \( \mu_{PCOX} = 150\mu m^2/V^2 \) and \( E_{CN} = 5V/\mu m, E_{CP} = 7V/\mu m \) (when considering velocity saturation). Do not ignore the internal capacitances of the network. To constrain your calculations, calculate the “worst-case” delay. For \( t_{pHL}(D-to-f) \), assume that C is LOW. For \( t_{pHL}(C-to-f) \), assume that A and B are LOW.

Problem #3
Assume that the maximum input capacitance of a chain of logic gates is 4fF and the capacitance at the output of the chain is 2.048pF. Assume that \( \beta = 2 \), \( k_{CG} = 2fF/\mu m \) and \( k_{CD} = 2fF/\mu m \).
(a) If the chain is composed of 4 inverters with \( W_P = 2W_N \), determine the appropriate sizing of each logic gate that minimizes delay.
(b) If the chain is composed of an arbitrary number of inverters, how many inverters (rounding down) and what is the fanout (sizing ratio for each stage)?
(c) If the chain is composed of ONLY 4 2-input NAND gates with \( W_P = W_N \), determine the appropriate sizing of each logic gate to minimize delay. Determine the effective fanout (as defined in class).

(d) If the chain is composed of 4 2-input NAND gates (as in part-c) and an arbitrary number of inverters, what is the optimal number of stages and the sizing for each stage?

(e) If the chain is composed of 4 2-input NOR gates with \( W_P = 4W_N \) and an arbitrary number of inverter, what is the optimal number of stages and the sizing for each stage?

**Problem #4**

Draw the stick diagram of the logic gate of Problem #2. Use no more than 2 layers of metal. Use the Line-of-Diffusion layout strategy described in class with the transistor widths running vertically and Metal-2 horizontally (and for power and ground). Bring in the inputs from the left on Metal-2 and output to the right on Metal-2.

**Project (Part 3)**

(a) Based on the sizing you chose of the last lecture, determine the rising and falling delay of \( C_{IN} \)-to-\( C_{OUT} \), \( C_{OUT}' \)-to-\( S_{OUT}' \), and \( C_{OUT}' \)-to-\( C_{OUT} \). To estimate the loading of the \( C_{OUT} \)-to-\( C_{OUT} \) delay, assume that \( C_{OUT} \) is also the \( C_{IN} \) of a second stage of the 1-bit adder. Assume \( k_{RN} = 12k\Omega \cdot \lambda \), \( k_{RP} = 30k\Omega \cdot \lambda \), and \( k_{CG} = 0.25fF/\lambda \), \( k_{CD} = 0.2fF/\lambda \) for both PMOS and NMOS. You may ignore velocity saturation.

(b) Draw the layout of the 1-bit adder cell. I suggest drawing three/four separate blocks. The \( C_{OUT}' \) logic, the \( S_{OUT}' \) logic, and the inverters. Start with the inverters since it is easier. Then you can combine them into a single 1-bit adder cell. Be sure to leave some room in the layout in case you decide to change the size of the devices. Use horizontal Metal-2 power and ground rail. I suggest roughly 100\( \lambda \) between power and ground. Run poly vertically (and hence use the layout style suggested in class). Assume that inputs \( G \) and \( P \) are from the left, and output \( S_{OUT} \) exits to the right. \( C_{IN} \) and \( C_{OUT} \) will be vertical signals (passing from one bit to the next as we will discuss later).

(c) Make sure that your layout matches your schematic and then run an IRSIM simulation based on your layout.