Homework 1

Name

Please refer to the material covered in the first lecture and the TI Reference Manual titled *TMS320C54x CPU and Peripherals (Reference Set 1)* for assistance in completing this assignment. You may need resources on the Internet to complete the Pentium 4 section.

**DSP/CPU Comparison.** Fill in the following table comparing relative characteristics of the two processors.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>TMS320C542</th>
<th>Pentium 4</th>
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<tbody>
<tr>
<td>Cost</td>
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<tr>
<td>Applications</td>
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<tr>
<td>Instruction width (bits)</td>
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<td>Speed (MHz)</td>
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<tr>
<td>Architecture</td>
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<td>Cache size(s), if any</td>
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<tr>
<td>Memory interface (on-chip or external)</td>
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<td>Interrupts (on-chip or external)</td>
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<td>Power dissipation in a ratio: mW/MIPS</td>
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</table>

**TMS320C54x Architecture.** Fill in the following blanks or explain as indicated.

1. Data/Program Buses.
There are three data buses, and which interconnect to various elements such as the CPU, data address generation logic, program address generation logic, on-chip peripherals and data memory. In addition, the program bus (PB) carries the instruction code and immediate operands from program memory.

2. Address Buses.
There are four address buses, , and to address page 0 (program memory) and page 1 (data memory) of the system memory.

3. Memory.
The DSP we are using has K of on-chip ROM, K of on-chip DARAM, and K of cache.

4. Data Arithmetic Logic Unit (Data ALU).
The data ALU performs all of the arithmetic and logical operations on data operands. It consists of:

(a) -bit central arithmetic unit.
(b) Two -bit accumulator registers.
(c) A parallel, single-cycle MAC.
(d) A barrel shifter.
(e) Data bus shifter/limiter circuits.
(f) Address Generation Logic (AGL). The AGL performs all of the address storage and address calculations necessary to indirectly address data operands in memory. It operates in parallel with other chip resources to minimize address generation overhead. The AGL has two identical address arithmetic units, PAGEN and DGEN, that can generate two -bit addresses every instruction cycle. The AGU consists of the following registers:

i. Auxiliary register arithmetic units: .
ii. Auxiliary registers: .

(g) Data buses.

5. Program Control Unit (PCU).
The program control unit performs instruction prefetch, instruction decoding, hardware loop control, and interrupt (or exception) processing. The -bit PC (program counter) can address 65,536 locations in program memory space. There are four mode and interrupt control pins that provide input to the program interrupt controller. Explain instruction prefetch:
Instruction Set Introduction. Refer to the TMS320C54x DSP Algebraic Instruction Set manual and class notes for the following questions.

1. Addressing Modes.
   The DSP instruction set contains a full set of operand addressing modes to access values. A value can be stored in three different places: __________, __________, and __________. The addressing mode determines how we access that value.