Electric Quick Start

Concepts
Electric is one of the many CAD tools available for circuit design. It is unique in its compact package unlike many of the more commonly used “industrial-strength” tools from Cadence Inc. or Mentor Graphics. Yet, it has maintained much of the capability of those tools. Most importantly, it is portable and free which makes it almost ideal for a classroom environment. The problem is that it is still under development. So, backup your work often to avoid significant loss of work due to crashes (File > Save).

The tool is based on facets. Each facet is a representation of a circuit. Any given circuit has many facets. For instance, the basic facets for a NAND gate are an icon (symbol representing the circuit, type ic in Electric), a symbolic transistor-based design (type sch), and a top-view layout of the mask layers (type lay). Other facets are possible for different types of simulation. When you create a circuit, there will likely be several facets for that circuit. The tool supports hierarchical design in which a circuit may contain sub-circuits. There are restrictions as to what can be embedded within a facet. A sub-circuit within a layout facet must be a layout. Meanwhile, a sub-circuit within a schematic facet is an icon. Hierarchy is traversed by pushing down and popping up between the hierarchical layers.

The tool must be explicitly connected. Some tools understand that there is an implicit connection between overlapping pieces of Metal-1, a M1-M2 Via, and Metal-2. This “implicit” understanding is often as a result of the tool performing “circuit extraction”. For better or worse, Electric does not behave this way. Contacts, vias, metals, and transistors have “ports” to which they must be connected. In order for the connection to be recognized, the connection must be explicitly indicated. It is useful to keep this characteristic in mind since it helps you to develop the right habits when using the tool.

The tool is lambda based. So channel length of devices cannot be smaller than $2\lambda$. The conversion from lambda to microns occurs behind the scene either with the appropriate model files for simulations or with the appropriate rules for mask generation.

Keyboard shortcuts are indicated to the right of a menu selection. Learning the shortcuts can improve your design speed significantly.

Getting Started
It is easiest to start by loading a library. This automatically sets the correct starting conditions such as mask process technology, schematic library, grid, simulation files, etc. File > Open Library – allows you to open the desired library. To create a facet, Facet > Edit Facet – allows you to edit a particular facet in your library (i.e. nand2{lay}) or you can click on New Facet to create a new facet.

Schematic Entry
While Electric supports “digital” schematics that allows you to incorporate built-in Inverters or And/Or functions, this class will only use “analog” schematics where you draw your circuit using either icons you have created or basic transistor/power/ground/resistor/capacitor symbols. Make sure that the technology is “analog” schematic by choosing Technology > Chang Current
Technology and selecting the schematic, analog. Notice that the components menu contains all the built-in components you are permitted.

Turning on a grid can help with aligning the schematic elements. Windows > Toggle > Grid.

Left-Click on the component-menu window selects the component. Left-Click on the schematics window drops an instance of the component. The circular object is the power symbol. The triangle is the ground symbol. Double-Click on a component brings up the component properties. You can specify the appropriate device size (based on lambda).

The ports between components need to be connected explicitly (do not assume any connection when placing them with overlap). Left-Click on a port of a component (i.e. the gate) and then Right-Click on another port would create a wire connecting the ports.

The input/output ports of this facet need to be defined. Left-Click on the end of a wire should automatically highlight the entire net and all its connections. Export > Create Export allows you to specify a name and a characteristic (Input or Output or both). These ports must be the same for the layout facet for the schematic to match the layout. You do not need to export power and ground.

Icons

A generic icon can be created using View > Make Icon. It is a box with the input and output pins. However, we often may want a more recognizable shape for standard symbols (XOR), or more unique symbols for special functions (ALU).

It is advisable to use 1-λ grid so that connections to the icons in future schematics are cleaner. Also, pay attention to the dimensions of the icon since consistent sizes make future schematics easier to read. Also, it might help visualizing connections to use a large icon for a large block.

You can either specifically edit the generic icon by choosing the icon from Facets > Edit Facets or use Facets > Down Hierarchy on the icon created in your schematics when you use View > Make Icon. The “artwork” components palette appears.

Place or move the Facet-Center (using Alt-Click) to where you want the reference point of the facet (see Layout Entry).

Arrows are created using Unfilled-Circles. The More option in the property dialog box (Double-Click the circle) allows you to specify the degrees that the arc spans. A line is cumbersome in Electric. An Open-Polygon can be edited using Edit > Special Function > Outline-Edit. You can only exit using the Quick-Key or using Exit-Outline-Edit in the same menu. Lines can only be edited in this fashion. However, arbitrary polygons are quite easy once this is mastered.

Make a habit of moving both the line and the exported name together when editing the icons. The line is also an Open-Polygon. Lastly, text can be added using “Text” in the component menu.

Layout Entry

It is a good idea to draw and simulate your schematic prior to embarking on layout of a gate. Make sure that you are using the correct technology library using Technology > Change Current Technology (mocmos is the basic MOSIS SCMS design rules). The technology’s lambda can be set as well using Technology > Change Units and set Lambda to the desired value (i.e. 0.12um for 0.25um technology rounded down). Technology > Technology Options can be used to select the correct adjustments to the rules (i.e. submicron) and the number of metal layers (i.e. 3). For convenience we will also set the alternate active and poly contact rules to keep things on lambda dimensions.

There are many default settings that can be changed. For instance, Arc > New Arc Options sets the default width for the connections (poly, metal, etc).
It is often easiest to start layout by looking at existing layout. It is not recommended that you use View > Make Layout. The lower left of the screen will display the type of component when you move your mouse over the components in the menu. It is also helpful to place a few of the items (similar to schematic entry) and Double-Click on them to see what options you have. Notice that stacks of overlapping layers are pre-made for you in the component menu i.e. transistors, and contacts. Layout is often easier when you show the grid using Windows > Toggle Grid. The grid size and snap can be adjusted using Windows > Grid Options and Alignment Options. We typically try to maintain a 1-λ grid although half-λ steps are possible use Edit > Move > Half-Arrow Key.

Design-Rule Checking (DRC) is built-in and is checking in the background incrementally. However, your layout is not guaranteed to be clean unless to do an explicit Tools > DRC > Hierarchical Check to recheck the entire facet and any sub-facets. The Messages window shows the errors. The errors are also highlighted on the layout. They can be navigated using the “>” and “<” keys. Note that the messages can be cryptic for beginning users. It is good to try a few simple cases to see and experience different errors. It is also useful to keep the design rule website handy to check the rules (www.mosis.org/Technical/Designrules/scmos/scmos-main.html). There are several different sets of rules. We will generally use the standard SCMOS rules for simplicity. While there may be a few inconsistencies, you need to fix all the violations specified by the Electric DRC.

Electric offers a 3-D view of your layout. It is often more fun than functional once you are accustomed to looking at layout. Windows > 3D Display > View in 3 Dimensions.

Transistors:
Widths are horizontal by default. The Edit menu contains many handy transform tools such as Rotate and Mirror. The size of the transistor can be adjusted by its property menu (through Double-Click). Edit > Duplicate is a handy option to replicate instead of Copy and Paste.

Contacts/Vias:
Diffusion/active contacts can be dropped next to transistors. You need to explicitly connect the diffusion with the contact similar to making connections in the schematics (select the source and Right-Click on the destination port). The metal layer must also be explicitly connected.

The same can be done for any inter-layer connection. Notice that the layer used for interconnect is the best guess based on the starting and ending ports. However, you can select the desired “routing” layer using the component menu. Also notice that when connecting between two different layers, Electric will automatically introduce a contact/via.

Wells:
Be sure to not forget to put a N/P-well contact for each cell you create. Metal1-N-Well-Con would be the contact connecting the N-Well of a PMOS transistor to VDD. Note that there are process technologies where the substrate is the P-Well instead of using an explicit P-Well. So even though we draw a P-Well, it may very well be ignored when we fabricate the transistors.

When we abut cells next to each other, the N/P-Well automatically defined with the transistors may not be what we want. There may be awkward gaps between cells that cause DRC errors. We can add a large piece of Well to cover all that we want using Edit > New Pure Layer Node and select N/P Well (this applies to any additional piece you want to add such as an additional piece of diffusion). The size of pure layer nodes can be changed by changing its property (Double-Click). It is often annoying that these pure layer nodes can be selected. So you can Edit > Selection > Make Selected Hard to make it more difficult to
select (you will need to use Alt+Click in order to select this layer). Edit > New Special Object > Coverage Implants can be used as well to automatically create hard-to-select pure layer nodes.

**Pins:**
Notice that you cannot draw a piece of interconnect without a starting port. So to draw a wire by itself, first drop a Pin, then the wire can be created as you would normally.

**Exports:**
You will need to match the export in your layout as in your schematics. The same Export > Create Export is used when the desired location is selected. Unique for layouts is that the location of the exports is a “pin” where ideally you will be connecting to the cell at a higher level of hierarchy. This means that you should make the exports at the edges of the layout or provide a higher level contact to make the “pin” easy to connect to. This may require you to draw some extra interconnect and select the edge. To make the selection easier, use Ctrl-Click to cycle through different possible selections for a location. "vdd" and "gnd" are recognized special nodes for power and ground so be sure to use it.

Layout can use cells that you have created to make layers with hierarchy. Cells can be included by use Edit > New Facet Instance (select what you want and Left-Click). Never create hierarchy by copying and pasting the layout. Changes in the original would not propagate.

The view of a lower level of hierarchy can be changed by selecting the instance and then Facet > Expand Facet Instance > (different options). Changes on a sub-cell is possible by pushing down into the sub-cell using Facet > Down Hierarchy (and/or In Place). The upper level can be returned in a similar fashion using Facet > Up Hierarchy.

When pushing two cells together, it may be necessary to place large areas of pure layer nodes of N/P-Wells to avoid DRC violations from the gaps and notches. Note that the higher level connections between cells are connected to the export locations.

The Facet-Center is an important location. Instead of being the actual center, it is a reference point. When you place the cell hierarchically, the Facet-Center is used as the location to which the rest of the cell is referenced. You can place the center using Edit > New Special Object > Facet Center. We nominally place it at the lower-left corner of the layout (excluding the wells). When the Facet-Center is already provided, it is by default Hard-to-Select. So you need to use Alt-Click to move it.

**Verification**
There are more steps in verification than just Design-Rules Checking (DRC). There are also Electrical-Rules Checking (ERC), and Network Consistency Checking (NCC). One of the key checks by ERC is to make sure that your wells are properly tied. NCC ensures that your layout matches your schematics. Since they are invoked often, you might want to Quick-Key them using Info > User Interface > Quick Key Options.

Both ERC and NCC are done after the DRC is clean. Tools > Electrical Rules > Analyze Wells – checks every P/N-Well has the correct connection to VDD or Gnd. It also reports the distance of these well-taps to transistors. Distances greater than 100λ deserve attention since it may cause “latchup”. The report also indicates the number of transistors. This should match your expectation.

NCC is useful to verify complex designs. The rationale is that your schematic is designed without error (after you’ve verified it with simulation). So all
you really need is to match the layout with the schematic. The problem is that NCC gives even more confounding messages than DRC.

Tools > Network > NCC Control and Options allows you to select which facets you want to compare. Set the dialog box for Recurse-Through-Hierarchy, Check-Export-Names, Check-Component-Sizes, and Ignore-Power-and-Ground. Click Do NCC. The result hopefully is “Facets XXX and YYY are equivalent (ZZZ seconds)”. Unfortunately, you may end up with differing layout and schematics and the NCC outputs must be interpreted.

Common errors are:
1. Only open the layout and schematic windows when doing NCC. That helps eliminate confusion.
2. Port names must agree. Note that series-stacked devices should have the same order (in how close each input is to the ground). Using “>” to scan through the errors is helpful here because it would indicate 2 errors where “NCC: Export names ‘xxx{sch}:b’ and ‘xxx{lay}:a’ do not match” and “NCC: Export names ‘xxx{sch}:a’ and ‘xxx{lay}:b’ do not match”.
3. Transistor sizes must agree.
4. You must export power and ground in your layout.
5. If you do not enable Ignore-Power-and-Ground it would result in an error. However the error can go away if you export power and ground in your schematics.

A very useful tool is NCC Preanalysis. All components and networks are listed as a result of the pre-analysis. Verbose and Graphics options can also help getting more information on the mismatches.

Switch-Level Simulation

Electric has two built-in switch-level simulators. ALS is not well-supported so we will focus on using IRSIM. Because it understands resistance and capacitances, it can estimate delay (remember that it does not take into account velocity saturation).

Tools > Simulation (Built-in) > Simulate should automatically run IRSIM. However, it is often best to verify the setting by checking Tools > Simulation (Built-in) > Simulation Options. IRSIM should be selected as the simulation engine. Verify the correct xxx.prm file is being used as the technology dependent model (parameter) file that contains the resistances, capacitances and lambda information.

If your nets have been exported correctly, it will see the net names that have been exported. All nodes are initialized without value (thick purple bar – undefined or floating). A primitive interface has been provided for graphical excitation of nodes. To set the value of an input, Left-Click on a node name, press “h” for digital 1, and “l” for digital “0”.

The simulator has 2 cursors. The cursor with no “x” is the primary cursor that indicates the time at which the input is switched. Dragging the cursor moves it in time. The second cursor (with “x”) is used to measure delay. Since control of the cursor is limited, you will not be able to achieve picosecond accuracy for the delay.

Windows > Adjust Position > Tile Vertically – allows arrangement of the windows so you can simultaneously see the simulation window and other windows. For schematic simulations, the color coding on the schematic is an indication of the value (magenta – “1”, blue – “0”, black – “x” an illegal value).

IRSIM has a much more extensive text-based interface.