Wires
Modern Interconnect

- 3 primary interconnect characteristics:
  - Capacitance
  - Resistance
  - Inductance
Capacitance

- Relationship between charge and voltage
  - Simple equation \((C = \varepsilon \text{area/distance})\) doesn’t apply any more.
- 2 or 3D field solvers to solve the capacitance between each conductor.
  - Create a big table for all possible configurations
- Capacitance Extraction
  - For every segment of each wire, look up from the table.
Impact of Interwire Capacitance

Capacitance is actually dominated by interwire capacitance within a layer.

- Between layer separation can be ~1μm. Within layer separation can be <0.2μm.
- width/thickness of metals are <<1

From: Bakoglu89
Examples of Permittivity ($\varepsilon$)

- **SiO$_2$** has very good permittivity.
  - Can’t reduce capacitance much more than a factor of 3
- Higher permittivity materials are used for gate oxide.

<table>
<thead>
<tr>
<th>Material</th>
<th>$\varepsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free space</td>
<td>1</td>
</tr>
<tr>
<td>Aerogels</td>
<td>~1.5</td>
</tr>
<tr>
<td>Polyimides (organic)</td>
<td>3-4</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>3.9</td>
</tr>
<tr>
<td>Glass-epoxy (PC board)</td>
<td>5</td>
</tr>
<tr>
<td>Silicon Nitride ($\text{Si}_3\text{N}_4$)</td>
<td>7.5</td>
</tr>
<tr>
<td>Alumina (package)</td>
<td>9.5</td>
</tr>
<tr>
<td>Silicon</td>
<td>11.7</td>
</tr>
</tbody>
</table>
Resistance

\[ R = \frac{\rho L}{H W} \]

Sheet Resistance \( R_0 \)

\[ R_1 = R_2 \]
Examples of Resistivity

- Typical material for wires is Aluminum
- Cu is used for higher level metals
  - Resistance improvement is <2x
- Poly and diffusion can be used as interconnect
  - Poly has ~100Ω/square
  - Diffusion has ~300Ω/square
  - Reduce resistance to 5Ω/square by using Al-Oxide (Silicide)

Contacts between layers are typically Tungsten and also has resistance.

<table>
<thead>
<tr>
<th>Material</th>
<th>ρ (Ω·m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver (Ag)</td>
<td>1.6 × 10⁻⁸</td>
</tr>
<tr>
<td>Copper (Cu)</td>
<td>1.7 × 10⁻⁸</td>
</tr>
<tr>
<td>Gold (Au)</td>
<td>2.2 × 10⁻⁸</td>
</tr>
<tr>
<td>Aluminum (Al)</td>
<td>2.7 × 10⁻⁸</td>
</tr>
<tr>
<td>Tungsten (W)</td>
<td>5.5 × 10⁻⁸</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Material</th>
<th>Sheet Resistance (Ω/☐)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n- or p-well diffusion</td>
<td>1000 – 1500</td>
</tr>
<tr>
<td>( n^+, p^+ ) diffusion</td>
<td>50 – 150</td>
</tr>
<tr>
<td>( n^+, p^+ ) diffusion with silicide</td>
<td>3 – 5</td>
</tr>
<tr>
<td>( n^+, p^+ ) polysilicon</td>
<td>150 – 200</td>
</tr>
<tr>
<td>( n^+, p^+ ) polysilicon with silicide</td>
<td>4 – 5</td>
</tr>
<tr>
<td>Aluminum</td>
<td>0.05 – 0.1</td>
</tr>
</tbody>
</table>

Textbook, pg. 145
Inductance

When signal is coupled to a ground plane, the current loop has an inductance.
- Approximate equation of a trace on a plane can be estimated.
- Too complex for simple equations and are part of field solvers.

Inductance is more apparent for upper layer metals
- Lower resistance and bigger current loop.
- Simple model (notice more nodes)

\[ L = \text{len} \frac{\mu_0}{2\pi} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \]
Modeling and Analysis
What Gates Drive

- Gate capacitance has scaled but not interconnects.
  - Impact of interconnects is quite significant.
- Wire model can be increasingly complex
  - Wire capacitance
  - Wire resistance
  - Wire inductance
- Resistive and Inductive modeling are distributed
  - Adds a lot of nodes to the analysis.
  - Transition time is no longer related to delay.
Examples of Wire Models

All-inclusive model

Capacitance-only
Wire Capacitive Modeling

- Reality: wire capacitance exists between conductors that are coupled.
- Simple model: 1st order
  - All capacitances are coupled to ground.
- Delay calculation
  - \[ C_{\text{total-load}} = C_{\text{self-loading}} + C_{\text{wire}} + C_{\text{gate-loading}} \]
- Model errors
  - Simultaneous transitions on adjacent wires.
  - Floating adjacent conductors
Capacitive Signal Coupling

Capacitance is sensitive to transition of coupled signal.
- Same direction: effective $C_{\text{couple}} = 0$
- Opposite directions: $C_{\text{couple}} = 2x$

Noise injection
- Capacitive coupling by an aggressor onto a victim
- If capacitances are driven by resistances, then the R’s impact the amount of noise.
- Example of a simple rule:
  - Consider noise when $R_{\text{aggressor}} < R_{\text{victim}}$

\[ \Delta V_1 = V_{DD} \]
\[ \Delta V_2 = \Delta V_1 \frac{C_1}{C_1 + C_2} \]

Charge conservation before and after the switching event.

[Sakurai 94]
Spectre’s Wire Capacitance

- Simple back of the envelope calculations – Zero\textsuperscript{th} order
  - 0.3fF/\textmu m – for minimum width wires
- Use capacitance extraction for better accuracy (2,2.5D Extractors)
- For each node (net)
  - Identify the geometry for each segment of wire
  - Determine the capacitance for the segment
    - Pattern matching (both node names AND geometry)
    - Table lookup and Extrapolation
  - Create a model for each net
    - Simple model (single capacitor per net)
    - Coupling model (capacitance > X is included between nets)
  - Computational cost is the criteria (LARGE # of nets to compute)
- Building capacitance table
  - Determine a set of common geometries.
    - Width of wire(s), spacing, upper/lower neighbors
  - Run 2,3-D electric field solver for the geometries (takes a LONG time)
Wire Resistance Modeling

- The resistance and capacitance of an interconnect are distributed.
  - The resistance distributes the capacitance into many nodes.
- Delay is different from a lumped model.
  - The result is roughly $\frac{1}{2}$ the delay.
  - For a step input:
    - $T_{\text{delay\_lumped}} = \ln(2) \cdot R \cdot C$
    - $T_{\text{delay\_distributed}} = 0.38 \cdot R \cdot C \sim \ln(2) \cdot R \cdot C / 2$
Elmore Delay and Π-Model

- Calculate Elmore delay of a chain of \( r, c \) (\( r = \frac{R_{wire}}{N} \), \( c = \frac{C_{wire}}{N} \))
  - Delay = \( 0.69^*\tau_{DN} \)
- About the same as splitting the total capacitance into 2, Π-model.

\[
\tau_{DN} = \left( \frac{L}{N} \right)^2 \left( r + 2rc + \ldots + Nrc \right) = \left( rcl^2 \right) \frac{N(N+1)}{2N^2} = RC \frac{N+1}{2N} \approx R \frac{C}{2}
\]
Extension of Elmore Delay

- Wires can have multiple destinations
  - Network is more complex.
  - Delay from X-to-Y is impacted by Z.
- Worst case approximation:
  - Lump all capacitance on Z to node N
  - Note second term.

\[
R_{\text{drv}} \left( C_{\text{self}} + \frac{C_w}{2} + \frac{C_w}{2} \right) + \\
R_{\text{drv}} \left( \frac{C_w}{2} + C_g \right) + \\
(R_{\text{drv}} + R_w) \left( \frac{C_w}{2} + C_g \right)
\]

\[t_{XY} = 0.69\]
Spectre’s RC Model

<table>
<thead>
<tr>
<th>Voltage Range</th>
<th>Lumped RC-network</th>
<th>Distributed RC-network</th>
</tr>
</thead>
<tbody>
<tr>
<td>0→50% ($t_p$)</td>
<td>0.69 RC</td>
<td>0.38 RC</td>
</tr>
<tr>
<td>0→63% ($\tau$)</td>
<td>RC</td>
<td>0.5 RC</td>
</tr>
<tr>
<td>10%→90% ($t_f$)</td>
<td>2.2 RC</td>
<td>0.9 RC</td>
</tr>
</tbody>
</table>

Step Response of Lumped and Distributed RC Networks:
Points of Interest.

\[ R \]
\[ C/2 \]
\[ R \]
\[ C/2 \]
\[ \pi \]
\[ R/2 \]
\[ R/2 \]
\[ C/4 \]
\[ C/2 \]
\[ C/2 \]
\[ \pi \]
\[ R/3 \]
\[ R/3 \]
\[ C/3 \]
\[ C/3 \]
\[ \pi \]
\[ R/6 \]
\[ R/3 \]
\[ C/3 \]
\[ C/3 \]
\[ \pi \]

\[ R/2 \]
\[ C \]
\[ T \]
\[ R/4 \]
\[ R/2 \]
\[ C/2 \]
\[ C/2 \]
\[ T2 \]
\[ R/6 \]
\[ R/3 \]
\[ C/3 \]
\[ C/3 \]
\[ T3 \]
Inductor Modeling

- The error is not very large so we won't be doing any in this class.
  - Ignored for most local nets.
- Care with “special” nets
  - Nets with precise delay needs
    - Especially over long distances
  - Nets with rise time requirements
    - Noise coupling is more severe with sharper edges.
- Common nets
  - Clock networks
    - Many latches work better with sharp clock edge ($t_{\text{setup}}$, data retention)
  - Wide and long data busses.
    - Noise coupling between busses.
Additional Problem: Mutual Inductance

- Magnetic flux couples to many signals
  - Not just to immediate adjacent signals (unlike capacitors.)
  - Coupling over a larger range.
  - Inductive noise (v=Ldi/dt)
    - Large di/dt due to fast signal transitions.
  - Sensitive to geometry and configuration.
  - Much bigger lump model
    - Matrix not sparse (coupling coefficient)
- Very big problem if we have to do this with every single signal.
  - Computationally, we know how, but too intensive.
Delay of RLC

- With a reasonably good transmission line
  - $R \ll$ than the line impedance.
    - Damping factor $\zeta \ll 1$
  - velocity = $\omega_0 = 1/\sqrt{LC}$
  - $t_{pd} = t_{flight} = \text{length} \times \sqrt{LC}$.

- With $\zeta$ near 1, the estimate can have large error
  - An empirical equation [Ismail & Friedman]

\[
\zeta = \frac{R}{2 \sqrt{\frac{C}{L}}}
\]

\[
t_{pd} = \left( \exp\left(-2.9\zeta^{1.35}\right) + 1.48\zeta \right) / \omega_n
\]
When Is Inductance Modeled

Two simple rule of thumbs are:

- Energy stored must be greater than energy lost
  - Long wires has large R thus no inductive effect.
- Signal rise-time must be smaller than propagation time.
  - Short wires has no inductive effect.
  - $t_{\text{rise/fall}} \sim 2 \times \text{delay}$ (without interconnect for worst-case)

\[ \frac{t_{\text{rise}(\text{fall})}}{2\sqrt{LC}} < \text{length} < \frac{2}{R\sqrt{LC}} \]