OUTLINE

REVIEW OF LAST LECTURES ...................................................................................................................... 2

INTRODUCTION TO THE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET) .......................................................................................................................... 3

History .................................................................................................................................................. 3
Advantages of the MOSFET Over BJT Devices .................................................................................... 3
MOSFET Device Principles ..................................................................................................................... 3
Qualitative Discussion of MOSFET Operation ..................................................................................... 4
The MOSFET Current Voltage Characteristics .................................................................................... 6

MOSFET TRANSISTOR CHARACTERISTICS ......................................................................................... 10

MOSFET TRANSISTOR CHARACTERISTICS ......................................................................................... 11

MOSFET TRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS .................................................. 13

MOSFET TRANSISTOR TERMINAL CURRENTS ..................................................................................... 16

MOSFET TRANSISTOR ENHANCEMENT AND DEPLETION MODE DEVICES ............................... 16

MOSFET TRANSISTOR BODY EFFECT ............................................................................................... 16

MOSFET TRANSISTOR OPERATING REGION ....................................................................................... 17

Cutoff .................................................................................................................................................. 17
Triode .................................................................................................................................................. 17
Saturation .......................................................................................................................................... 17

MOSFET SMALL SIGNAL CHARACTERISTICS ................................................................................... 17

MOSFET SMALL SIGNAL MODEL ......................................................................................................... 20
REVIEW OF LAST LECTURES

- Introduction to Amplifier and Amplifier Principles
- Nonlinear microelectronic devices: introduction
  - Semiconductor junction diodes
    - Semiconductor junction diode circuit analysis
    - Semiconductor junction diode: small signal behavior
  - Semiconductor junction diode applications
  - Semiconductor junction technology and principles
  - Semiconductor Junction Diode in Reverse Bias
- Semiconductor Bipolar Junction Transistor
  - Structure
  - Principles
  - Introduction to Current Voltage Characteristics
  - The Motivation for Bias Point Design
  - Bias Point Analysis
  - Small Signal Properties
- BJT Small Signal Model
  - BJT Common Emitter Amplifier
    - Small Signal Analysis
  - BJT Common Emitter Amplifier with Emitter Degeneration
    - Small Signal Analysis
  - BJT Common Base Amplifier
    - Small Signal Analysis
  - BJT Common Collector Amplifier
    - Small Signal Analysis
INTRODUCTION TO THE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

HISTORY
- The Bipolar Junction Transistor (invented by Bardeen, Brattain, and Shockley and his team at AT&T) is generally regarded as the first transistor.
- However, the first transistor was first conceived in 1926 by Lilienfeld. His concept was to modulate the conductivity of a material by application of an electric field.
- Early attempts to control the electric field internal to a semiconductor crystal by external means met with failure.
- Bardeen learned that crystal surfaces, when formed, carry defects known as surface states. Specifically, surface electronic structure can support a high density of electrons that create an electrostatic shield between the external environment and the internal material.
- However, the AT&T team ultimately developed the bipolar junction transistor along with the understanding of minority carrier transport by Shockley.
- In the late 1950’s, following investigation of the nature of insulating SiO₂ formed by gas-phase oxidation, the field effect transistor was invented.
- This entered production in the 1960s, enabling modern digital microelectronics.

ADVANTAGES OF THE MOSFET OVER BJT DEVICES
- We have seen that the BJT provides high gain. However, its input resistance, $r_π$, is low.
- Also, the BJT occupies large on an integrated circuit system
- The MOSFET device offers the advantages of nearly infinite DC input resistance.
- Further, the MOSFET structure is compact and may be scaled to nanometer dimensions.
- The BJT and MOSFET differ fundamentally:
- The BJT relies on the injection, transport, and collection of minority carriers
- The MOSFET is a majority carrier device.

MOSFET DEVICE PRINCIPLES
- A cross-sectional, schematic view of the MOSFET transistor is shown above.
The MOSFET relies on the Field Effect phenomenon. Here, the application of an external field penetrates the semiconductor, altering the electron and hole potential energy profile. With application of sufficient field, the conductivity of the semiconductor surface can be altered from an insulating character to a metallic conductivity with a change in device resistance of over 10 orders of magnitude in a time scale measured in picoseconds.

Application of the intense electric field required (10^6 to 10^7 V/cm) hindered early development.

However, the naturally occurring SiO₂ dielectric at the Si surface is one of the most effective insulators known. It provides ideal, defect-free properties at thicknesses of only several molecular layers.

The MOSFET has four important terminals (although, we will be largely concerned with only three).

These are the Source, Drain, and Gate terminals, shown above, and the Body terminal associated with the substrates.

The implementation of the complete transistor systems will appear as below:

![Diagram of MOSFET](image)

**Figure 2. Complimentary NMOS and PMOS (CMOS) Transistors**

**QUALITATIVE DISCUSSION OF MOSFET OPERATION**

Now, we can first discuss the most important principles of MOSFET operation.

First consider the structure below with MOSFET terminals operating at the same potential

![Diagram of NMOS and PMOS with V_DS = 0 and V_GS = 0](image)

**Figure 3. NMOS and PMOS Transistor with V_DS = 0 and V_GS = 0**

Now, we observe that two p-n junctions exist in series between Source and Drain. Effectively infinite resistance appears between Source and Drain.
Now, if we apply a positive potential to the Gate, relative to Source, \( V_{GS} > 0 \), then we may induce a channel for electron conductivity by reducing electron potential energy in the region of the Gate Insulator-Si Substrate interface. This channel will be occupied by electrons populating this from the flanking, heavily doped n\(^+\) Source and Drain regions.

![Figure 4. Formation of a channel with \( V_{GS} > 0 \)](image)

- Conduction may now occur from Source to Drain via the Channel.
- Now, applying increasing Gate potential, increases the channel depth.

![Figure 5. The NMOS channel depth increases with increasing \( V_{DS} \)](image)

- Now, consider the application of a voltage between Drain and Source with Drain Positive.
- There will be a voltage drop along the channel due to current flow in the channel. This will reduce the potential difference between Gate and Channel. Thus, the depth of the channel will be reduced near the Drain.

![Figure 6. The NMOS channel is reduced in depth near the Drain for increasing \( V_{DS} \)](image)

- Now, as we further increase \( V_{DS} \) we will reach a condition referred to as *Saturation* where the
channel depth reaches zero at the Drain and the channel is said to be in “pinch-off”.

- This is the Saturation Voltage, or $V_{DS_{Sat}}$

- As $V_{DS}$ is increased above $V_{DS_{Sat}}$, the channel characteristic is not changed, the voltage drop along the channel is not changed, and channel current remains nearly independent of $V_{DS}$.

- Note that there is an unfortunate terminology usage. *Saturation operation for a MOSFET corresponds to BJT Active Region operation.*

**THE MOSFET CURRENT VOLTAGE CHARACTERISTICS**

- Now, the Gate and Channel form a parallel plate capacitor
- A minimum voltage exists, referred to as a Threshold Voltage, $V_t$, that when applied to the Gate relative to the substrate, will form a conducting channel. It depends on the capacitance between Gate and substrate. Capacitance per unit area is $C_{OX} = \frac{\varepsilon_{OX}\varepsilon_0}{t_{OX}}$ where, $t_{OX}$ is the Gate oxide thickness and $\varepsilon_{OX}$ is the oxide dielectric constant.

- Now, the Threshold Voltage, $V_t$ is:
  $$V_t = \phi_{MS} + 2\phi_F + \frac{Q_b}{C_{OX}} + \frac{Q_{SS}}{C_{OX}}$$

- Where, $\phi_{MS}$, is the fundamental work function difference between the Gate and Substrate materials, $\phi_F$ is the difference in Fermi level potential between the inverted surface with its channel and bulk Silicon. $Q_b$ is the depletion layer charge that must be accumulated to enable a channel, and $Q_{SS}$ is the trapped charge at the Si/SiO$_2$ interface.

- There exists an electric field between Gate and Channel that is determined by the applied bias, $V_{GS}$ and $V_t$.

- The potential difference between Gate and Source is reduced by application of a voltage, $V_{DS}$.

- Since the potential drop along the channel varies linearly with distance, the average potential difference is reduced by $V_{DS}/2$

- Now, for a Channel of Width, $W$, and Length, $L$, the capacitance will be
  $$C_{OX} = \frac{\varepsilon_{OX}\varepsilon_0WL}{t_{OX}}$$

- Further, the charge stored in the Channel is, therefore
Now, the current flow is equal to the total charge induced in the channel divided by the time required for the action of the electric field to sweep this charge from Source to Drain.

This time is the transit time,

$$\tau_{SD} = \frac{L}{v_e}$$

Where \( v_e \) is the electron drift velocity defined through mobility as,

$$v_e = \mu_e E_{DS}$$

Where \( E_{DS} \) is the electric field between Drain and Source. Now, this, in turn is

$$E_{DS} = \frac{V_{DS}}{L}$$

So, finally,

$$\tau_{SD} = \frac{L^2}{\mu_e V_{DS}}$$

Now, the Drain to Source current is

$$i_{DS} = \frac{Q_c}{\tau_{SD}} = \frac{e_{OX}e_0\mu_e V_{DS}}{t_{OX}} \left( \frac{W}{L} \right) \left( V_{GS} - V_t \right) - \frac{V_{DS}}{2} = \frac{e_{OX}e_0\mu_e}{t_{OX}} \left( \frac{W}{L} \right) \left( V_{GS} - V_t \right) V_{DS} - \frac{V_{DS}^2}{2}$$

And, this can also be written as

$$i_{DS} = \mu_e C_{OX} \left( \frac{W}{L} \right) \left( V_{GS} - V_t \right) V_{DS} - \frac{V_{DS}^2}{2}$$

Now, this is only valid for

$$V_{DS} < (V_{GS} - V_t)$$

This defines the MOSFET Triode operating region.

Now, pinch-off occurs when

$$V_{DS} = (V_{GS} - V_t)$$

For voltages greater than \( V_{DS} = (V_{GS} - V_t) \), the current remains constant (since the channel field and shape remains constant as Drain-Source voltage increases).

So, we can obtain this current by substituting \( V_{DS} = (V_{GS} - V_t) \) and

$$i_{DS} = \frac{\mu_e C_{OX}}{2} \left( \frac{W}{L} \right) (V_{GS} - V_t)^2$$

For NMOS transistors we will define a constant, \( k_n \).
\[ k_n' = \mu_n C_{OX} \]

and

\[ k_p' = \mu_p C_{OX} \]

So that now, in the Saturation region:

\[ i_{DS} = \frac{k_n'}{2} \left( \frac{W}{L} \right) (v_{GS} - V_t)^2 \]

And in the Triode region

\[ i_{DS} = k_n' \left( \frac{W}{L} \right) \left[ (v_{GS} - V_t) v_{DS} - \frac{v_{DS}^2}{2} \right] \]

The typical characteristics of state-of-the-art MOSFET technology are:

- \( V_t \): 0.2 – 0.8 V (NMOS enhancement mode devices)
- \( V_t \): (-0.2) – (-0.8 V) (PMOS enhancement mode devices)
- \( L \): 0.08 – 0.25 \( \mu \) m
- \( W \): 0.2 – 200 \( \mu \) m
- \( \varepsilon_{OX} \): 3.97
- \( t_{OX} \): 20 – 50 nm
- \( \mu_e \): 580 cm\(^2\)/V-s
- \( \mu_h \): 230 cm\(^2\)/V-s
- \( k_n' \): 10 – 200 \( \mu A/V^2 \)
- \( k_n' \): 4 – 80 \( \mu A/V^2 \)

The MOSFET transistor symbol is drawn as:

\[ \text{Figure 7. (left) The NMOS Transistor and (right) PMOS Transistor} \]

- The MOSFET transistor structure is well-adapted to integrated circuit fabrication.
- Complex circuits are readily implemented with compact devices.
- Also, NMOS and PMOS complimentary devices may be paired to form switching (large signal circuits) that operate at low energy. Examples of the CMOS inverter, two inverters in series, and their corresponding “standard cell” layout are shown below.
Figure 8. Schematic CMOS Inverter shown at left with its integrated circuit standard cell, below. At right, two inverters operating in series are shown in schematic view and with their standard cell implementation.

Figure 9. CMOS Integrated circuit imaged by Scanning Electron Microscope after removal of insulating oxide layers - exposing conductor network. (From IBM Microelectronics)
MOSFET TRANSISTOR CHARACTERISTICS

- For NMOS transistors:
  \[ k_n = \mu_e C_{\text{OX}} \]

- Saturation region:
  \[ i_{DS} = \frac{k_n}{2} \left( \frac{W}{L} \right) (v_{GS} - V_t)^2 \]

- And,
  \[ i_{DS} = k_n \left( \frac{W}{L} \right) \left[ (v_{GS} - V_t) v_{DS} - \frac{v_{DS}^2}{2} \right] \]

- Triode region
  \[ i_{DS} = k_n \left( \frac{W}{L} \right) \left[ (v_{GS} - V_t) v_{DS} - \frac{v_{DS}^2}{2} \right] \]

- For PMOS transistors:
  \[ k_p = \mu_h C_{\text{OX}} \]

- Saturation region:
  \[ i_{DS} = \frac{k_p}{2} \left( \frac{W}{L} \right) (v_{GS} - V_t)^2 \]

  \[ i_d = \frac{k_p}{2} \left( \frac{W}{L} \right) (v_{GS} - V_t)^2 \left( 1 + \lambda v_{DS} \right) \]

- Note \( v_{DS}, v_{GS}, \) and \( V_t \) will all be negative

- Triode region
  \[ i_{DS} = k_p \left( \frac{W}{L} \right) \left[ (v_{GS} - V_t) v_{DS} - \frac{v_{DS}^2}{2} \right] \]

- The typical characteristics of state of the art MOSFET technology is:
  - \( V_t: \) 0.2 – 0.8V (NMOS enhancement mode devices)
  - \( V_i: \) (-0.2) – (-0.8V) (PMOS enhancement mode devices)
  - \( L: \) 0.08 – 0.25\( \mu \)
  - \( W: \) 0.2 - 200\( \mu \)
  - \( \varepsilon_{\text{OX}}: \) 3.97
  - \( t_{\text{OX}}: \) 20 – 50 nm
  - \( \mu_e: \) 580 cm\(^2\)/V-s
  - \( \mu_h: \) 230 cm\(^2\)/V-s
The MOSFET transistor symbol is drawn as:

![MOSFET symbols](image)

**Figure 10.** (left) The NMOS Transistor and (right) PMOS Transistor

### MOSFET Transistor Characteristics

- The MOSFET characteristics vary according to its Operating Region. Operating Regions for the MOSFET are analogous to those of the BJT. *Please note the duplication in the definition of the Saturation Region between MOSFET and BJT.*

<table>
<thead>
<tr>
<th></th>
<th>Saturation</th>
<th>Triode</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NMOS</strong></td>
<td>$v_{GS} \geq V_t$</td>
<td>$v_{DS} \geq v_{GS} - V_t$</td>
</tr>
<tr>
<td><strong>PMOS</strong></td>
<td>$v_{GS} \leq V_t$</td>
<td>$v_{DS} \leq v_{GS} - V_t$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Cutoff</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NMOS</strong></td>
<td>$v_{GS} &lt; V_t$</td>
</tr>
<tr>
<td><strong>PMOS</strong></td>
<td>$v_{GS} &gt; V_t$</td>
</tr>
</tbody>
</table>

- Compare with BJT

<table>
<thead>
<tr>
<th></th>
<th>Active</th>
<th>Saturation</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NPN BJT</strong></td>
<td>$v_{BE} \geq 0.7$</td>
<td>$v_{CB} \geq 0$</td>
</tr>
<tr>
<td><strong>PNP BJT</strong></td>
<td>$v_{EB} \geq 0.7$</td>
<td>$v_{BC} \geq 0$</td>
</tr>
</tbody>
</table>
• Now, we can examine the Current –Voltage Characteristics.
• First, we can examine the dependence of Drain Current on Gate-Source potential difference for fixed Drain-Source Voltage.
• Now, we can also examine the characteristics of this amplifier for various Gate-Source potential difference values and for varying Drain-Source voltage.
• Note the similarity of this characteristic to the BJT. However, note that whereas the BJT displayed an exponential Base-Emitter Voltage– Collector Current characteristic, the MOSFET shows a square-law dependence between Gate-Source Voltage and Drain-Source Current.
• There is a major simplification in the operation and analysis of the MOSFET over the BJT:
  a. Gate current is zero
  b. Drain Current equals Source Current
• Also, as for the BJT, if we examine the Current-Voltage Characteristic, we observe a slope in the Characteristic with an increase in Drain Current, \( i_D \), with increasing Drain-Source voltage, \( v_{DS} \).
• This is described with the equation:
  \[
  i_D = \frac{k_n W}{2L} (V_{GS} - V_t)^2 \left( 1 + \lambda v_{DS} \right)
  \]
  where \( \lambda \) is the channel length modulation parameter
• Note also that we now simply denote Drain-Source current as \( i_D \)
• A resistance is associated with this current-voltage characteristic. This is analogous to the BJT output resistance.

  \[
  r_O \equiv \frac{1}{\frac{\partial i_D}{\partial v_{DS}}}_{v_{GS} = \text{Constant}}
  \]
  \[
  r_O = \frac{1}{\lambda k_n \frac{W}{2L} (V_{GS} - V_t)^2} \approx \frac{1}{\lambda I_D}
  \]
  where \( I_D \) is the DC Bias Drain Current value.
• Also, sometimes, the channel length modulation parameter is described by an Early Voltage. With
  \[
  \lambda = \frac{1}{V_A}
  \]
  \[
  r_O \approx \frac{V_A}{I_D}
  \]
MOSFET TRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS

- One of the most important features of MOSFET technology is the inherent ability to produce transistors having response controlled by design of the transistor geometry, the ratio of W/L.
- For digital application, the channel length, L, may often be designed at its lowest value, to achieve the smallest, highest gain, and highest speed response.
- In many analog applications, minimum L values may not be ideal.
- However, for both cases, we can tune transistor response by selection of W/L.
- Now, we can examine the MOSFET current voltage characteristics. First, we will pick a transistor for which we have:
  - $V_t = 0.4 \text{ V}$, $k_n' = 0.1 \text{mA/V}^2$, $L = 0.2 \mu \text{m}$, $W = 10 \mu \text{m}$, $\lambda = 0.01 \text{V}^{-1}$
  - We will use this PSpice circuit model

![Figure 11. A NMOS circuit used for computing the $I_D - V_{GS}$ characteristic. The PSpice model parameters are $V_T = 0.4$ $K_P = 100 \mu \text{m} \cdot \text{V}, L = 0.2 \mu \text{m}, W = 10 \mu \text{m}, \lambda = 0.01 \text{V}^{-1}$](image)

- The response is shown below. Try computing Drain Current at $V_{GS} = 1.4 \text{ V}$, where $(V_{GS} - V_t) = 1 \text{ V}$. Compare this with the PSpice result.

![Figure 12. The NMOS transistor Drain Current - Gate-Source-Voltage Characteristic. Note the square-law response.](image)

- Now, let's perform the same analysis below, using a PMOS transistor as shown.
Figure 13. A PMOS circuit used for computing the $I_D - V_{GS}$ characteristic. The PSpice parameters are $V_{TO}=-0.4$ \ KP=100\mu \ L=0.2\mu \ W=10\mu \ lambda=-0.01$

Figure 14. The results of the $I_D - V_{GS}$ characteristic for PSpice model parameters are $V_{TO}=0.4$ \ KP=100\mu \ L=0.2\mu \ W=100\mu \ lambda=0.01$

- Now, to demonstrate the effects of W/L variation, we will select a new transistor geometry. This will include $W = 100\mu$, and $L = 0.2\mu$. Then, we observe:
Now, in the application of the MOSFET to amplifier systems, the output voltage swing at the Drain may be large.

So, we must examine the Drain current – Drain-Source-Voltage characteristic. This is shown below for $V_t = 0.4 \text{ V}$, $k_n = 0.1 \text{mA/V}^2$, $L = 0.2 \mu\text{m}$, $W = 10 \mu\text{m}$, $\lambda = 0.01 \text{V}^{-1}$

Now, for this analysis, we sweep $V_{DS}$ while adjusting $V_{GS}$ with 10 values of $V_{GS}$ from 0 to 2V in steps of 0.2V.

---

**Figure 15. The NMOS Drain current – Drain-Source-Voltage characteristic**
- Examine this characteristic and find the family of points where $V_{DS} = (V_{GS} - V_t)$ (the point where the transistor enters Saturation).
- Each of the current characteristics above shows a linear dependence on $V_{DS}$. This is the channel length modulation behavior, discussed above.

---

**Figure 16. The NMOS Drain current – Drain-Source-Voltage characteristic – showing the Early effect.** The channel length modulation parameter, $\lambda$, is 0.01 for this transistor. Thus, the Early voltage ($V_A = \lambda^{-1}$) = 100V.
• This behavior is described by the introduction of the Early voltage and the _channel length modulation parameter_, \( \lambda \).

**MOSFET TRANSISTOR TERMINAL CURRENTS**

• Now, we recall that for the BJT, Emitter current was the sum of Base and Collector currents.
• For the MOSFET, current at the Gate terminal is zero! (The Gate oxide is an insulator).
• Thus, Drain and Source current are equal.
• This simplifies bias analysis dramatically, since we do not require that we account for Base Current.
• We must also recognize, however, that a voltage drop (analogous to \( V_{BE} = 0.7 \) for an NPN transistor) may not be invoked for the MOSFET. This requires a modified approach for Bias Point calculation.

**MOSFET TRANSISTOR ENHANCEMENT AND DEPLETION MODE DEVICES**

• We will later discuss a modification to the MOSFET device that permits another mode of operation, Depletion Mode.
• The MOSFET channel for the devices we have discussed, is doped at low density to be p-type for NMOS devices and n-type for PMOS devices. The channel region is “inverted” by application of the Gate potential. This is referred to as an “enhancement” device since application of Gate potential enhances conductance in the channel.
• But, the MOSFET channel may be “implanted” (dopant atoms may be implanted by directing a beam of high energy ions on the silicon surface). In this case, n-type dopants may be introduced into the channel of an NMOS device.
• This creates a channel at a reduced threshold voltage for an NMOS device.
• Thus, while \( V_t \) was positive in the range of 0.2 – 0.8V for typical technology systems, this may now be negative. \( V_t \) may be as large as –1V.
• Thus, a channel exists at \( \Delta V_{GS} = 0V \).
• Then, the Depletion mode device may be operated where application of Gate voltage may reduce or deplete the channel.

**MOSFET TRANSISTOR BODY EFFECT**

• The Body Effect will be discussed more fully, later. Here is a brief discussion now.
• In the MOSFET structure, the channel for conduction is formed in the substrate between Source and Drain regions.
• Now, for typical circuits, a large potential difference of up to several volts may exist between the Source and Drain regions and the substrate. These junctions are reverse biased. However, as the voltage between Source and substrate are increased, the voltage required to form a channel also increases.
• Thus, threshold voltage, $V_t$, depends on substrate voltage.
• We will discuss this later in the context of analog and digital device applications

MOSFET TRANSISTOR OPERATING REGION

CUTOFF
• In the Cutoff Region, no channel is present, and the MOSFET transistor shows very high resistance between Source and Drain. This may be utilized to form a high resistance switch device with Cutoff (off-state) resistance greater than $10^{10} \Omega$
• The MOSFET may operate in the Cutoff region in digital logic applications.

TRIODE
• The MOSFET operates in the Triode region when $V_{DS}$ is very small. This occurs in digital logic applications.
• In the Triode Region, the MOSFET may be placed in a bias condition that allows it to operate as a voltage controlled resistor.
• In the MOSFET Triode region the transistor characteristic is

$$i_{DS} = k_p \left( \frac{W}{L} \right) \left( V_{GS} - V_t \right) V_{DS} - \frac{V_{DS}^2}{2}$$

• Note that for small $V_{DS}$ this characteristic is linear and a resistance can be defined.
• This enables the MOSFET to be employed as a voltage-controlled, linear resistor (see Problem 5.15)

SATURATION
• Here the MOSFET characteristics “saturate” in the pinchoff region as $V_{DS}$ increases above $V_{DS} = (V_{GS} - V_t)$
• This is the region in which we operate the MOSFET as an amplifier, as we will discuss next.

MOSFET SMALL SIGNAL CHARACTERISTICS

• Now, the non-linear characteristic of the MOSFET transistor provides desired gain.
• However, as for the BJT, this non-linear characteristic requires that we design amplifier systems to accept and process small amplitude signals such that the non-linear nature of the transistor amplifier does not produce distortion.
• As for the BJT, the MOSFET transistor produces an output current modulation for an input voltage modulation.
• For the BJT, we observed a small signal current, $i_d(t)$ for an input small signal voltage, $v_{bc}(t)$
• This was modeled as a transconductance.
• Now, as for the BJT, the MOSFET transistor has an associated value of transconductance, $g_m$
To review, let's consider the MOSFET Drain current.

\[ i_D = \frac{k_n}{2} \left( \frac{W}{L} \right) \left( v_{GS} - V_t \right)^2 \left( 1 + \lambda v_{DS} \right) \]

Now, this can be described as the sum of DC and time dependent components.

\[ i_D = I_D + i_d \]

And there will be a corresponding sum of DC and time dependent components for Gate-Source voltage.

\[ v_{GS} = V_{GS} + v_{gs} \]

We can consider the limit of \( \lambda = 0 \).

Then, also let's substitute this small signal voltage into our expression for Drain current.

\[ i_D = \frac{k_n}{2} \left( \frac{W}{L} \right) \left( V_{GS} - V_t + v_{gs}(t) \right)^2 = \frac{k_n}{2} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_t)^2 + v_{gs}^2(t) + 2(V_{GS} - V_t)v_{gs}(t) \right] \]

Gathering DC and time dependent terms

\[ i_D = \frac{k_n}{2} \left( \frac{W}{L} \right) \left( V_{GS} - V_t \right)^2 + \frac{k_n}{2} \left( \frac{W}{L} \right) \left[ v_{gs}^2(t) + 2(V_{GS} - V_t)v_{gs}(t) \right] \]

We can identify the DC component:

\[ I_D = \frac{k_n}{2} \left( \frac{W}{L} \right) \left( V_{GS} - V_t \right)^2 \]

and the small signal component as well. We can consider the limit of small \( v_{gs} \) where,

\[ v_{gs} \ll (V_{GS} - V_t) \]

Then,

\[ i_d = \frac{k_n}{2} \left( \frac{W}{L} \right) \left( v_{gs}^2(t) + 2(V_{GS} - V_t)v_{gs}(t) \right) \equiv \frac{k_n}{2} \left( \frac{W}{L} \right) \left[ (2(V_{GS} - V_t))v_{gs}(t) \right] \]

We can see that this in the form of a transconductance

\[ i_d = g_m v_{gs}(t) \]

with

\[ g_m = \frac{k_n}{2} \left( \frac{W}{2L} \right) \left( 2(V_{GS} - V_t) \right) = k_n \left( \frac{W}{L} \right) (V_{GS} - V_t) \]

Now, this can also be written,

\[ g_m = 2 \sqrt{\frac{k_n}{2} \left( \frac{W}{L} \right)} I_D = 2k_n \left( \frac{W}{L} \right) I_D \]

Further, using,
\[
\frac{2I_D}{k_n' \left( \frac{W}{L} \right) \left( V_{GS} - V_t \right)^2} = \left[ \left( V_{GS} - V_t \right)^2 \right]
\]

- Then,

\[
g_m = \frac{2I_D}{V_{GS} - V_T}
\]

- Let's consider a demonstration. The circuit below uses the same transistor parameters that have been used to generate the characteristics above. Note that \( V_{DS} = 5V \). The small signal Gate-Source voltage is 10mV amplitude.

- Using our expression above for Drain current, with \( V_t = 0.4V \), \( k_n' = 0.1mA/V^2 \), \( L = 0.2\mu \), \( W = 10\mu \), \( \lambda = 0.01V^{-1} \), we see that Drain current will be 2.625mA at \( V_{DS} = 5V \).

- This is in agreement with the PSpice analysis.

**Figure 17.** Transistor amplifier demonstrating MOSFET small signal transconductance.

- For application of a 10mV amplitude signal, we obtain a current amplitude of 0.0525mA. This is a modulation superimposed on the 2.625mA signal.
Figure 18. The PSpice result for Drain current for the above amplifier. Note that a current signal of about 0.052mA amplitude is superimposed on a 2.625mA DC current.

- We can compute the transconductance value. This is 5.12 mA/V
- At a 10mV amplitude, we expect a small signal current of
  \[ i_d = g_m v_{gs} = 5.12 \text{mA/V}(10\text{mV}) = 0.0512 \text{mA} \]
- This is in good agreement with the PSpice result.

MOSFET SMALL SIGNAL MODEL

- Just as for Diode and BJT circuits, we see that we can always decompose signals into components that are time independent and time dependent.
- We see that for all of the Diode, BJT, and MOSFET devices, the current-voltage characteristics of our circuits will be described by two independent equations.
  - c. In the time-independent (DC) equation, we see that time dependent, small signal sources are not present (they are replaced by their zero equivalents).
  - d. In the time-dependent (small signal) equation, we see that time independent, DC signal sources are not present (they are replaced by their zero equivalents).
- Thus, a circuit model for the transistor small signal behavior may be introduced. This is a hybrid-\( \pi \) model.
- The hybrid-\( \pi \) model for NMOS and PMOS transistors ignoring the small signal output resistance, \( r_o \), is:

![Hybrid-\( \pi \) model without output resistance]

- The hybrid-\( \pi \) model for NMOS and PMOS transistors including the small signal output resistance, \( r_o \), is:

![Hybrid-\( \pi \) model with output resistance]

- Our next topic of discussion will be MOSFET Bias Design and Analysis.