A Frequency-Agile Single-Chip QAM Modulator with Beamforming Diversity

Kyung-Ho Cho, Member, IEEE, and Henry Samueli, Fellow, IEEE

Abstract—Architecture and circuit design techniques for VLSI implementation of a single-chip quadrature amplitude modulation (QAM) modulator with frequency agility and antenna beamforming characteristics are presented. In order to achieve reliable wireless communication modem function, the single chip all-digital QAM modulator implements various features, including high data rates with bandwidth efficiency, flexibility, meeting a wide variety of user throughput requirements with variable and width and data rates in a multi-user system, and robustness, incorporating diversity and redundancy techniques to guarantee robust communication for various operating environments. The modulator components consist of several digital processing building blocks, including various finite-impulse-response (FIR) filters, an innovative variable interpolation filter, a four-channel frequency translator with quadrature mixer for antenna beamforming diversity, a quadrature direct digital frequency synthesizer (QDDFS), a numerically controlled oscillator (NCO), a QAM formatter, a pseudorandom noise (PN) generator, an \( x/\sin x \) filter, and a microcontroller interface. An optimized architecture and chip implementation for the variable modulator is derived and evaluated which will support symbol rates from 6 kBaud to 8.75 MBaud continuously and digitally flexible IF frequencies up to 70 MHz with four-channel antenna beamforming function.

Index Terms—Antenna beamforming diversity, DDFS, FIR filter, half band filter, frequency agility, modulator, Nyquist filter, polynomial interpolator, QAM, variable rate interpolator, VLSI, wireless modem.

I. INTRODUCTION

Over the last decade, both wired and wireless broadband communication technologies have made significant advances, especially the recent introduction of broadband services over high-speed digital subscriber lines or cable demonstrates increasing consumer demand for virtually instantaneous access to a large volumes of information. In order to enable anytime and anywhere access without a wired infrastructure, future communication systems are expected to be able to provide the same level of service over the air using wireless technology. In addition, recent technology innovation in circuits and devices, the availability of license-free frequency bands, and user needs for communication with portable devices have been key factors leading to the introduction of wireless communication products. However, to achieve reliable wireless communication at high data rates (tens of megabits per second) in the harsh and dynamic wireless environment, a number of challenging technical problems will be encountered. The solution to this problem often requires sophisticated techniques including bandwidth-efficient modulation, equalization, and diversity techniques in space, time, or frequency.

The Wireless and Adaptive Mobile Information Systems (WAMIS) project of University of California at Los Angeles (UCLA) proposes a wireless modem design operating within the unlicensed 2.4-GHz ISM band, having various features: 1) adaptability, providing maximum performance for the diverse channel conditions; 2) high data rates with bandwidth efficiency, meaning tens of megabits per second rates, comparable to existing wired technologies; 3) flexibility, meeting a wide variety of user throughput requirements with variable bandwidth and data rates in multi-user system; and 4) robustness, incorporating diversity and redundancy techniques to guarantee robust communication for various operating environments. The WAMIS modem consists of an analog front-end (RF section) and an all-digital intermediate frequency (IF) and baseband [1]. The development of the all-digital modem consists of two parts, a transmitter and a receiver. This paper focuses on the integrated circuit implementation of the modulator that will be the digital part of the transmitter.

In order to meet the critical design requirement mentioned above, several considerations are reflected in the transmitter architecture. First, the \( M \)-ary quadrature amplitude modulation (QAM) technique, well-known as a bandwidth-efficient modulation scheme, is exploited. In this design, six different QAM modulation constellations from 4 to 256 are implemented to accommodate adaptive bit allocation. Next, in order to increase flexibility, two architectural uniquenesses are exploited in two different frequency domains, baseband and IF band frequency. In the baseband domain, an innovative interpolation scheme is adopted to provide an incommensurate symbol rate change, called baseband frequency-agility. In addition, by implementing a digital IF frequency QAM modulation architecture using a direct digital frequency synthesizer (DDFS), digitally flexible IF frequency-agility from 0 to 70 MHz can be obtained.

Communicating at these high transmission rates over the harsh wireless environment results in the problem of multipath ISI due to frequency-selective fading. Hence, the realization of low error-rate transmission requires measures to avoid the performance degradation due to signal fading and ISI. An equalizer using a digital filter can compensate for multipath fading in the temporal domain, while an antenna array can be usually employed to control beamforming in the spatial domain. The combination of diversity reception and equalization can provide significant reduction in ISI [2]. Therefore, to improve diversity...
and redundancy, the WAMIS modem employs four-channel antenna beamforming diversity in the transmitter and adaptive antenna combining in the receiver to electronically steer the radio signal toward the desired source and place nulls in the direction of interferers. Table I summarizes the main features of frequency-agile QAM modulator.

### II. CHIP ARCHITECTURE

#### A. System Overview

A frequency-agile single chip QAM modulator is shown in Fig. 1. This modem architecture incorporates many unique features required for a reliable wireless modem. First, in order to achieve spectral efficiency, it exploits an all-digital QAM modulation architecture which has advantages over the traditional analog QAM implementation [3]. In addition, the architecture implements a digital sampling function not only in baseband frequency but also in the intermediate frequency (IF) band which can achieve perfect amplitude and phase matching characteristics in the quadrature mixing operation. In particular, this modulator allows the off-chip digital-to-analog converters (DACs) to operate at a fixed sampling clock rate. Therefore, all necessary sampling rate conversion must be accomplished through a unique digital interpolation scheme which allows symbol rates to be continuous. In general, the input data rates and output clock rates may be incommensurate. This interpolation scheme implements the baseband frequency-agility characteristic which allows more flexibility to the modem. The single-chip modulator accepts external parallel and serial input data streams or can generate a training signal using a pseudo-noise (PN) generator implemented by a 16-bit programmable linear feedback shift register. All necessary initial and coefficient values of the shift register can be set by the microcontroller interface circuit. Then the input stream is optionally differential-quadrant and Gray encoded before being mapped to the desired QAM constellations (4 to 256 QAM) in order to resolve the phase ambiguity arising in the receiver and to minimize the probability of bit errors. After the pulse shaping function with 15% square-root-Nyquist filtering at two samples per symbol, the signal is polynomially interpolated up to the output sampling rate. The single complex signal is then transferred to four complex coefficients multipliers which implement the four-channel antenna beamforming diversity in the spatial domain. Four mixers and a quadrature direct digital frequency synthesizer (QDDFS) up-convert the complex baseband beamformer outputs to a user programmable IF frequency of up to 70 MHz which accomplish the IF frequency-agility. The four real signals are then optionally filtered by an \( x/\sin(x) \) filter to compensate for digital-to-analog converter frequency distortion and delivered to four off-chip digital-to-analog converters.

#### B. System Design (Architecture Considerations)

1) **Variable Rate Interpolator**: The programmable interpolation filter is the most complex component in the QAM modulator and its performance affects significantly the overall performance of the QAM modulator. It is known that a dedicated interpolation function unit is more efficient than the conventional cascaded multistage interpolation to implement a wide range of interpolation ratios [4]. Three typical dedicated interpolator architectures are considered in this design: a cascaded-integrator-comb structure (CIC), a recirculating half-band finite-impulse-response (FIR) filter structure, and a polynomial-based variable interpolator. The CIC interpolator structure is simple because it does not require any multipliers [5]. Therefore, it is well suited to high-sampling-rate conversion architectures, but it suffers from some limitations. One limitation is the requirement for a second stage lowpass filter to compensate for the passband droop introduced by the \( \sin(Lx)/\sin(x) \) roll-off characteristic of the CIC filter. Also, with this CIC structure, the achievable conversion ratio is limited to an integer value only. On the other hand, the recirculating half-band FIR filter is a hardware-efficient structure by time-sharing a single interpolate/decimate-by-two half-band filter. However, the recirculating half-band FIR filter structure also suffers from an inherent

---

**Table I: Main Features of QAM Modulator**

<table>
<thead>
<tr>
<th>System Feature</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spectral Efficiency</td>
<td>4-, 16-, 32-, 64-, 128-, 256-QAM</td>
</tr>
<tr>
<td>Frequency Agility</td>
<td>Variable Symbol Rate and IF frequency</td>
</tr>
<tr>
<td>Spatial Diversity</td>
<td>4-Channel Adaptive Antenna Beamforming</td>
</tr>
<tr>
<td>Convenient Control</td>
<td>Real-Time Control By Microprocessor</td>
</tr>
<tr>
<td>High Integration</td>
<td>Bit Stream Input Data --- Digital IF Output</td>
</tr>
</tbody>
</table>
performance limit in that the conversion ratio is limited to only the powers-of-two values [3].

As pointed out early, the dedicated interpolation methods considered so far have restricted conversion ratios to an integer or powers-of-two values. For these cases, the output sampling is always synchronized to the input sampling. This means the available interpolation ratio is limited to a rational number. Therefore, with the previous two structures, it is not feasible to achieve irrational interpolation ratios. One way to overcome this problem is to employ a polynomial-based interpolation to calculate the sampling value of the interpolated signal [6], [7].

In this polynomial interpolator, the available interpolation ratio can be an irrational value. Therefore, the possible conversion ratio is said to be continuously variable. Because of this conversion ratio flexibility, the polynomial interpolator structure is chosen as the dedicated interpolator structure for this QAM modulator.

2) Implementation of Frequency-Agility Using Polynomial Interpolator: Depending on the type of polynomial, the performance and hardware complexity of the modulator are different. In order to examine their effects on the modulator design and determine which type of the interpolator is appropriate, two criteria are considered: desired throughput and hardware complexity. These ideas are discussed in the following section in detail.

a) Performance Consideration: Fig. 2 shows a block diagram for a MATLAB system level simulation used to simulate the performance tradeoffs in the total QAM modulator. It is known that the $\sin(x)/x$ frequency response of the polynomial interpolator generates the signal and image at integer multiples of the input sampling rate and the rejection of the signal images in the variable interpolator depends on the relative bandwidth of the signal at the input signal [6]. Therefore, a multistage upsampling block in Fig. 2 is designed to compensate the imperfection in the frequency response of the polynomial interpolator by increasing the amounts of pre-oversampling ratios before the polynomial interpolator stages.

The reference throughput for the system performance is set at a 50-dB signal-to-noise-ratio (SNR) threshold, where the SNR is defined by the ratio of the power of hard decisions to the power of the errors between the hard and soft decisions in a receiver model. Several factors were considered in determining the final modulator architecture: 1) the type of polynomial used in the interpolator and 2) the number of pre-oversampling ratios which compensate for the imperfections in the image rejection characteristics of the polynomial interpolator. From system simulation, two different types of polynomial interpolators, linear and piecewise parabolic, and 8 or 16 of pre-oversampling ratios are selected for hardware complexity considerations [8].

b) Hardware Complexity Consideration: The maximum operating frequency of this design is determined by the required maximum IF frequency and any additional frequency margin required for the band-pass filter after the digital-to-analog (DAC) converter. The maximum IF frequency required assumed to be 70 MHz with a 10-MHz symbol rate. The additional frequency margin strongly depends on the characteristic of the available analog band pass filter. By considering these factors and using the well-known Nyquist sampling criterion, 200 MHz is determined as the maximum required sampling frequency. Out of several possible hardware efficient structures [9], based on the consideration of hardware complexity of the two interpolators and the number of pre-oversampling ratios, piecewise parabolic interpolators with eight-times pre-oversampling is chosen as a final QAM modulator architecture.

3) Detail Upsampling Architecture: As shown in Fig. 3, because of the imperfection of frequency characteristic in polynomial interpolator, eight-times pre-oversampling stages are required. The eight-times oversampling is implemented by the two-times inherent sampling ratio in the square root Nyquist filter and by two hardware-efficient half-band filters with 15 and 7 taps. The 59-tap square-root Nyquist filter with a 15% excess bandwidth factor is also used as a signal shaping filter to minimize intersymbol interference (ISI) at the receiver. On the other hand, the two half-band filters are used to remove image signals from the previous fixed two-times upsampling stages. The polynomial interpolator then takes eight-times oversampled data as an input and produces oversampled output data at the same rate as the system clock frequency (the modulator’s highest sampling rate). Depending on the sampling ratio at the interpolation stage, the symbol rate (signal bandwidth) will be flexible enough to satisfy the system requirement of adaptive bit and symbol selection [8].

4) Antenna Beamforming Diversity: It is reported that in the indoor environment, a single-tap diversity combiner with decision-feedback equalization performs well [2]. In practice, however, determining an acceptable number of antenna branches and equalization taps is important in order to provide desired performance. As described, the baseband digital signal processor chips developed as part of the UCLA wireless modem project are a single-chip modulator and a single-chip
demodulator. The modulator design is based on results obtained in the transceiver system simulation. A four-element antenna combiner is considered as a compromise between performance and hardware complexity, and simulations demonstrate that a four-channel antenna provides a significant performance improvement when compared to a single-antenna system [2].

In order to implement four-channel antenna diversity, the variable interpolator output is split into parallel data paths, each of which will be multiplied by its own unique complex-valued coefficients. This operation can be viewed as a complex multiplication operation as follows:

$$Y = (Y_I + jY_Q) = X \cdot H = (X_I + jX_Q)(H_I + jH_Q)$$

where $Y$ is the output of the multiplier, $X$ is the interpolator output signal, and $H$ is the complex antenna beamforming coefficient. The straightforward implementation of the product uses four real multipliers and two adders to compute the real ($Y_I$) and imaginary components ($Y_Q$).

$$Y_I = X_I H_I - X_Q H_Q$$

$$Y_Q = X_Q H_I - X_I H_Q.$$

III. VLSI IMPLEMENTATION

A. FIR Filter

There are three FIR filter blocks in the QAM modulator: 1) a 59-tap square-root Nyquist filter; 2) a 15-tap halfband filter; and 3) a 7-tap halfband filter. All three blocks have a built-in two-times upsampling function. For a dedicated application, the FIR structure that produces sufficient throughput with the lowest complexity is desired. In order to achieve reduced hardware complexity, a fixed coefficient set is used rather than a set of coefficients with programmability. One of the typical methods used to achieve this reduction is the canonic-signed digit (CSD) method [10]. This results in a multiplierless filter so that a hardware-efficient implementation is possible. In addition, the coefficient symmetry characteristic of linear phase FIR filter can also be exploited to save chip area by sharing multipliers between the symmetric taps.

There are numerous other architectural optimization techniques to reduce the hardware complexity in the FIR filter design. First, interleaving the data samples in time can allow a single filter core to calculate two or more filter responses. When multiple paths use the same filter coefficients to process different data, this interleaving technique is very efficient. In the QAM modulator, the square-root Nyquist filter and the half-band filters must process both $I$ and $Q$ data streams. Therefore, the interleaving technique is implemented in the square-root Nyquist and 15-tap halfband filters. This results in a more efficient layout with only a minor penalty in a slightly increased power dissipation.

Utilizing the fact that the input and output data rates in the FIR filters always differ by a factor of two in this design, a simple and elegant structure [11], called a polyphase structure, can be derived which divides the filters into two sub-filters (even, odd) and allows a half-rate operating frequency within each subfilter. Since interpolation involves zero padding between samples, the output data is the convolution of the input data alternatively with the even taps and the odd taps as shown in Fig. 4. This makes it possible to divide an interpolate-by-two filter into two subfilters with the even and odd taps. A two-to-one multiplexer is placed at the output, through which data from each subfilter are alternatively selected to form the interpolated and filtered output data stream. As a result, only the output multiplexer needs to operate at the output sample rate, while the rest of the filter operates at one-half the output sample rate.

Fig. 5 shows a low data rate signal processing block implemented by the hardware efficient structure. Because the 7-tap filter stage does not use the interleaving technique, it consists of two identical polyphase structures for the $I$ and $Q$ rails.

B. Multiplier

The basic multiplier used in this QAM modulator design is a parallel array multiplier architecture which utilizes Booth encoding and a carry-save partial product reduction scheme [12]. There are three different multipliers used to implement the multipliy-accumulator ($8 \times 16$) in the variable interpolator, the antenna beamforming function ($12 \times 12$), and the frequency translator ($10 \times 16$) from baseband to the IF frequency band. Because the minimum speed performance required is 200 MHz, one stage of the pipeline structure is inserted into all the multiplier arrays. After exploiting the one-stage pipeline, the final
critical path delay of the 8×16, 12×12, and 10×16 is improved to be 2, 3, and 3 ns, respectively.

C. Piecewise-Parabolic Polynomial Interpolator

Fig. 6 illustrates the piecewise-parabolic polynomial interpolator. This block diagram shows a special case of the general Farrow structure [13] with \( \alpha = 0.5 \). Because power-of-two multiplications are implemented as bit-shifts in hardware, the hardware implementation is simple and efficient. The interpolator block can be divided into three parts: 1) numerically controlled-oscillator (NCO) which supplies the control signal \( \mu_k \) and eight-times symbol clock reference (Bclk8); 2) the front transversal filter in the Farrow structure; and 3) the multiply–accumulate block in the Farrow structure.

1) Numerically Controlled-Oscillator (NCO): An NCO can be implemented with a digital accumulator (ACC), which is simply a two-input adder followed by a register whose output is fed back to one adder input. The rectangular output waveform of the most significant bit (MSB) is one of the important NCO outputs which can be used as an eight-times symbol clock reference (Bclk8). The other input to the ACC is the frequency control word (FCW) from the microcontroller interface. The block diagram of the NCO and example output waveforms are drawn in Fig. 7. It contains a 32-bit one-stage pipelined accumulator which consists of two 16-bit carry–select adders and operates above 200 MHz. The MSB output of the register is selected as Bclk8, which is a clock corresponding to \( T_s \), the input symbol time duration. Also, the seven most significant bits of the 32-bit NCO output are used as the variable interpolator fractional interval, \( \mu_k \). The frequency control word (FCW) of the NCO is controlled by the microcontroller interface block, which allows FCW data to be easily changed during modulation operation.

2) Farrow Structure Implementation of Piecewise-Parabolic Interpolator: As shown in Fig. 6, the front transversal filter of the variable interpolator is exactly the same as the structure of a direct form FIR filter. Fig. 6 shows an implementation of the filter using carry–save addition with a carry–select adder used as a vector-merge addition (VMA) at the output stage. The expected maximum operating speed for this block is 100 MHz which is exactly half of the maximum sampling rate. Because the critical path delay is less than 10 ns, four consecutive carry–save adders can be connected without a pipeline stage. The filter coefficients with powers-of-two values result in only shift-and-add operations for the coefficient multiplication rather than real multiplications. This results in significant area savings. The remaining blocks, operating at the maximum clock speed of 200 MHz, are the 16×8 high-speed multiplier and an adder.

D. Frequency Translator with Four-Channel Beamforming Diversity

1) Antenna Beamforming Multiplication: The antenna beamforming multiplication (Fig. 8) consists of four multipliers with 12×12 input coefficients and two four-input adders. The target operating speed of this block is 200 MHz. In order to accomplish this speed performance, a multiplier with one pipeline stage and a high-speed adder using carry–save addition are used. Implementation with one carry–save adder is not possible because the number of inputs to the adder are four. Therefore, a two-stage carry–save adder is required. Because the critical path delay for the adder is larger than 5 ns (200 MHz), one pipeline stage is inserted between the carry–save adder and the carry–select adder. In this design, the wordlength is 12 bits for the signal input data and antenna beamforming coefficients, while the internal signal wordlength is 16 bits.
2) Frequency Mixing:

a) QDDFS: The architecture used for the QDDFS utilizes an overflowing phase accumulator to generate the phase argument of the sine function generator [14]. That generator is a ROM look-up table storing samples of the sine waveform. The design of the QDDFS is based on the work reported in [15] and [16], where ROM compression techniques resulted in a substantial complexity reduction.

b) Four-Channel Frequency Mixing: The four-channel frequency mixing blocks consist of one QDDFS, eight multipliers with 16×10 bits input coefficients, and four adders as shown in Fig. 9. The adder and multiplier structures in the frequency mixing blocks are exactly the same as the one used for complex coefficient multiplication except for the number of input bits. The addition function is implemented using a carry-save adder with one pipeline stage.

E. X/Sin x Filter

A 7-tap x/sin x filter is used to precompensate for the distortion from the zero-order hold characteristic of the subsequent D/A converter. The amount of compensation is approximately 3 dB at the half sampling frequency. Since the output sampling rate of the modulator is expected to be up to 200 MHz, the architecture based on the folded transposed direct form with carry-save and carry-select addition was used. Fig. 10 shows the hardware implementation of the 7-tap x/sin x FIR filter in the folded transposed direct form. In order to decrease the input loading effect in the folded transposed direct form FIR filter, the MSB sign extension is replaced with a compensation vector (CV) [17]. In this design, as shown in Fig. 10, the final modulator output is 10 bits.

F. Peripheral Blocks

The peripheral functions include a microprocessor controller interface, a PN generator for a training sequence and built-in-self-test (BIST) signal generation, a serial-to-parallel data stream converter, and a QAM signal formatter (symbol mapper) which supports various formats from 4 to 256 QAM encoded with two different schemes.

IV. DESIGN VERIFICATION

A system board was designed for testing and monitoring the spectral performance as shown in Fig. 11. As mentioned earlier, the single-chip modulator needs programmed control signals which decide the operation of internal blocks such as the frequency control words for the NCO and QDDFS, the antenna beamforming coefficients, and the selection of various QAM modes and input signals. These control signals are provided by a commercial pattern generator (HP 16 500A). In addition, the master clock signal is supplied from a dedicated pulse generator which generates two complementary (clk and clkb) signals for the DUT and a 10-bit D/A converter. In order to observe the spectrum of the output waveform, digital outputs from the modulator must be converted into analog signals by the D/A converter. Finally, a spectrum analyzer is used to monitor the spectra of various outputs from the D/A converter.

The single-chip QAM modulator has several important features including a variable symbol rate, as well as the flexibility of IF center frequency. In this test configuration, the input data source used is assumed to be the built-in PN-signal. In order to evaluate the all features, several performances are checked under various speed conditions: 1) a typical output spectrum with maximum symbol rate and IF center frequency; 2) a group of different output spectra from baseband subblocks; 3) a group
Fig. 13. Block diagram used for internal spectrum measurement.

Fig. 14. Frequency spectrum of internal baseband blocks. (a) Square-root Nyquist filter. (b) 15-tap halfband filter. (c) 7-tap halfband filter. (d) Variable interpolator.

of spectra with variable symbol rates; and finally 4) a group of spectra with various IF center frequencies.

Fig. 12 illustrates a typical output spectrum of an IF center frequency modulated signal. This spectrum of the frequency translator output is measured at the master clock frequency of 140 MHz with a symbol rate of 8.75 MHz and an IF center frequency of 70 MHz.

By controlling the bypass mode register in the microcontroller interface circuit, the internal spectrum of each function block can be observed. A simplified block diagram used for internal spectrum measurement is shown in Fig. 13. With the master clock frequency of 159 MHz, the output sampling frequencies of the block are 19.75, 39.75, 79, and 159 MHz for the four clocks shown. The achieved symbol rate under these conditions is 9.875 MHz. Fig. 14 illustrates corresponding spectra of each internal block. In Fig. 14(a), which shows the spectrum of the square-root Nyquist filter output, the sampling rate of the signal is 19.75 MHz so that all the image signals are repeated at multiples of this rate. Because the output signal is measured by the D/A converter operating at 39.5 MHz, all the image signals are attenuated by the \( \sin x/x \) envelope characteristic of the D/A converter. Similarly, in the 15-tap filter [Fig. 14(b)], the images are seen to be repeated at 39.5 and 79 MHz. For the 7-tap halfband filter and the variable interpolator, the same expected image signals can be observed as shown in Fig. 14(c) and (d). From these results, it can be concluded that the baseband block is working at clock frequency of 159 MHz.

The variable symbol rate is another important feature of this the single-chip QAM modulator. The required symbol rate can be changed by simply changing the frequency control word (FCW) of the NCO. Fig. 15 shows typical examples of output spectrum of the variable interpolator with four different symbol rates of 1.25, 5.0, 5.5734, and 10 MBaud. These spectra are measured at the master clock rate of 158 MHz.

The digitally controlled flexible IF center frequency is also another important characteristic of the single-chip modulator.
In order to show this characteristic, four different IF center frequencies (70, 78.5, 80, and 90 MHz) are illustrated in Fig. 16 with different symbol rates. In addition, as shown in Fig. 16, the minimum 43-dB measured stopband attenuation of the modu-
lated signal spectrum can be achieved for all QAM constellations. The stopband attenuation based upon system level simulation was about 65 dB [8].

In addition, the target functions confirmed were as follows: 1) various QAM modes (4, 16, 32, 64, 128, and 256 QAM); 2) two different QAM formats, differential-quadrant and Gray encoding; 3) three different input data formats (serial, parallel, and PN-signal); and 4) the four-channel antenna beamforming diversity function.

V. CONCLUSION

A development of a low-cost and broadband wireless modem with spatial diversity is the primary goal of the UCLA wireless modem project. The modem exploits several communication system techniques to allow maximum flexibility and reliability while providing high data rates. In order to realize flexible data rates and high bandwidth efficiency, the modem uses the quadrature amplitude modulation (QAM) technique. In the spatial domain, this modem employs antenna beamforming in the transmitter and adaptive antenna combining in the receiver. The development of architectures and circuit design techniques for VLSI implementation of a single-chip all-digital QAM modulator with variable symbol rates and flexible digital intermediate frequency (IF) is the primary interest of this paper.

This paper focuses on demonstrating a new architecture for a dedicated variable rate polynomial-based interpolator and developing an all-digital frequency-agile single-chip QAM modulator. The single-chip modulator consists of several fixed-coefficient FIR filters, an innovative variable interpolator using a polynomial structure, a four-channel frequency translator for antenna beamforming diversity, a PN-generator for the BIST signal and the training sequence generation, a quadrature direct digital frequency synthesizer (QDDFS) for orthogonal signal (sine and cosine) generation, a selectable $x/\sin x$ filter for DAC distortion, and a microcontroller interface compatible with a commercial microcontroller (Motorola HC11).

Functional testing of the single-chip modulator chip indicates that all targeted functions with different QAM modes and input modes perform well. Tables II and III illustrate a summary of the single-chip QAM modulator features and measured performances.

Measurement of power dissipation ranges from 1.15 to 1.82 W as a function of the symbol rate at a power supply voltage of 3.3 V and 70 MHz IF center frequency. The entire modulator operates during this test, including the four-channel frequency translator, the variable interpolator, the NCO, the QDDFS, and all FIR filters. The master clock frequency is fixed at 140 MHz and the variable symbol rates are controlled by adjusting the frequency control word.

The final chip photograph (Fig. 17) has a total chip area including a pad ring of 63.84 mm$^2$ using a 0.6-$\mu$m triple metal
CMOS process. The total transistor counts are 430 000 and the package is 132-lead pin grid array.

ACKNOWLEDGMENT

The authors would like to thank to J. S. Putnam and E. Roth for many technical discussions and their support.

REFERENCES


Kyung-Ho Cho (M’93) received the B.S. and M.S. degrees in control and instrumentation engineering from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering with emphasis in integrated circuits and systems from the University of California, Los Angeles (UCLA) in 1999.

He joined LG Electronics (formerly Goldstar Electronics) Central Research Laboratories, Seoul, in 1984, where he was primarily engaged in the design of integrated circuits for consumer electronics using bipolar technologies. From 1986 to 1988 he was a Co-op Engineer in the analog integrated circuit design group of Hitachi Takasaki Works, Takasaki, Gunma, Japan, where he was involved in the design and development of audio power amplifier circuitry. From 1989 to 1992 he was a Section Manager of the IC design and development group of LG Semiconductor, Seoul. His group was involved in the design of high-power driver ICs for motor and LCD panels. From 1993 to 1999 he was a Research Assistant in the Electrical Engineering Department at UCLA, where his research interest was in the field of CMOS integrated circuit and system design using digital signal processing and communication system theory for high-speed data communications systems. In 1999, he was a Consultant with Lucent Technologies, Huntington Beach, CA, where he was involved in the design of integrated circuitry for digital broadcast systems. Since 2000 he has been a Senior Member of Technical Staff with Cognet Microsystems, Los Angeles, CA, where he has been involved in the design of high data rate communication circuits for optical fiber systems. His research interests include high-speed and low-power integrated circuit design for digital communication applications.

Henry Samuei (S’75–M’79–SM’99–F’00) was born in Buffalo, NY, on September 20, 1954. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of California, Los Angeles (UCLA), in 1975, 1976, and 1980, respectively.

From 1980 to 1985 he was with TRW, Inc., Redondo Beach, CA, where he was a Section Manager in the Digital Processing Laboratory of the Electronics and Technology Division. From 1980 to 1985 he was also a part-time Instructor in the Electrical Engineering Department at UCLA. In 1985 he joined UCLA full-time, where he is currently a Professor in the Electrical Engineering Department. His research interests include the areas of digital signal processing, communications systems engineering, and CMOS integrated circuit design for applications in high-speed data transmission systems. In 1988 he co-founded PairGain Technologies, Inc., Tustin, CA, a telecommunications equipment manufacturer, and in 1991 he co-founded Broadcom Corporation, Irvine, CA, an integrated circuit supplier to the broadband communications industry. Since 1995 he has been on leave of absence from UCLA while serving full-time as Chief Technical Officer of Broadcom where he is responsible for all research and development activities for the company.

Dr. Samuei is the recipient of the 1988/1989 TRW Excellence in Teaching Award of the UCLA School of Engineering and Applied Science, the Meritorious Paper Award of the 1991 Government Microcircuit Applications Conference, the 1995 Best Paper Award from the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and the Jack Kilby Best Paper Award from the 2000 IEEE International Solid-State Circuits Conference. He received the 1999 Engineer of the Year Award from the Orange County Section of the IEEE, and the 2000 IEEE Circuits and Systems Society Industrial Pioneer Award. In 2000 he was elected a Fellow of the IEEE “for contributions to VLSI architectures and realizations for high bit-rate digital communication systems.”