1. Actual op amps exhibit “nonlinear” characteristics. For example, the voltage gain may be equal to 1000 for $-1 \text{ V} < V_{\text{out}} < +1 \text{ V}$, 500 for $1 \text{ V} < |V_{\text{out}}| < 2 \text{ V}$, and close to zero for $|V_{\text{out}}| > 2 \text{ V}$.

(a) Plot the input/output characteristic of this op amp.

(b) What is the largest input swing that the op amp can sense without producing “distortion” (i.e., nonlinearity)?

2. An op amp exhibits the following nonlinear characteristic:

$$V_{\text{out}} = \alpha \tanh[\beta(V_{\text{in}1} - V_{\text{in}2})].$$

(8.113)

Sketch this characteristic and determine the small-signal gain of the op amp in the vicinity of $V_{\text{in}1} - V_{\text{in}2} \approx 0$.

3. A noninverting amplifier employs an op amp having a nominal gain of 2000 to achieve a nominal closed-loop gain of 8. Determine the gain error.

4. A noninverting amplifier must provide a nominal gain of 4 with a gain error of 0.1%. Compute the minimum required op amp gain.

5. Looking at Equation (8.11), an adventurous student decides that it is possible to achieve a zero gain error with a finite $A_0$ if $R_2/(R_1 + R_2)$ is slightly adjusted from its nominal value.

(a) Suppose a nominal closed-loop gain of $\alpha_1$ is required. How should $R_2/(R_1 + R_2)$ be chosen?

(b) With the value obtained in (a), determine the gain error if $A_0$ drops to $0.6A_0$.

6. A noninverting amplifier incorporates an op amp having an input impedance of $R_{\text{in}}$. Modeling the op amp as shown in Fig. 8.44, determine the closed-loop gain and input impedance. What happens if $A_0 \rightarrow \infty$?

7. A noninverting amplifier employs an op amp with a finite output impedance, $R_{\text{out}}$. Representing the op amp as depicted in Fig. 8.45, compute the closed-loop gain and output impedance. What happens if $A_0 \rightarrow \infty$?

8. In the noninverting amplifier shown in Fig. 8.46, resistor $R_2$ deviates from its nominal value by $\Delta R$. Calculate the gain error of the circuit if $\Delta R/R_2 \ll 1$. 

9. The input/output characteristic of an op amp can be approximated by the piecewise-linear behavior illustrated in Fig. 8.47, where the gain drops from $A_0$ to $0.8A_0$ and eventually to zero as $|V_{in1} - V_{in2}|$ increases. Suppose this op amp is used in a noninverting amplifier with a nominal gain of 5. Plot the closed-loop input/output characteristic of the circuit. (Note that

![Figure 8.46.](image)

![Figure 8.47.](image)
the closed-loop gain experiences much less variation; i.e., the closed-loop current is much more linear.)

10. A truck weighing station incorporates a sensor whose resistance varies linearly with the weight: \( R_S = R_0 + \alpha W \). Here \( R_0 \) is a constant value, \( \alpha \) a proportionality factor, and \( W \) the weight of each truck. Suppose \( R_S \) plays the role of \( R_2 \) in the noninverting amplifier (Fig. 8.48). Also, \( V_{in} = 1 \) V. Determine the gain of the system, defined as the change in \( V_{out} \) for a given change in \( W \).

11. Calculate the closed-loop gain of the noninverting amplifier shown in Fig. 8.49 if \( A_0 = \infty \). Verify that the result reduces to expected values if \( R_1 \to 0 \) or \( R_3 \to 0 \).

12. An inverting amplifier must provide a nominal gain of 8 with a gain error of 0.2%. Determine the minimum required op amp gain.

13. The op amp used in an inverting amplifier exhibits a finite input impedance, \( R_{in} \). Modeling the op amp as shown in Fig. 8.44, determine the closed-loop gain and input impedance.

14. An inverting amplifier employs an op amp having an output impedance of \( R_{out} \). Modeling the op amp as depicted in Fig. 8.45, compute the closed-loop gain and output impedance.
15. An inverting amplifier must provide an input impedance of approximately 10 kΩ and a nominal gain of 4. If the op amp exhibits an open-loop gain of 1000 and an output impedance of 1 kΩ, determine the gain error.

16. An inverting amplifier is designed for a nominal gain of 8 and a gain error of 0.1% using an op amp that exhibits an output impedance of 2 kΩ. If the input impedance of the circuit must be equal to approximately 1 kΩ, calculate the required open-loop gain of the op amp.

17. Assuming $A_0 = \infty$, compute the closed-loop gain of the inverting amplifier shown in Fig. 8.50. Verify that the result reduces to expected values if $R_1 \rightarrow 0$ or $R_3 \rightarrow 0$.

![Figure 8.50.](image)

18. Determine the closed-loop gain of the circuit depicted in Fig. 8.51 if $A_0 = \infty$.

![Figure 8.51.](image)

19. The integrator of Fig. 8.52 senses an input signal given by $V_{in} = V_{out} \sin \omega t$. Determine the output signal amplitude if $A_0 = \infty$.

20. The integrator of Fig. 8.52 is used to amplify a sinusoidal input by a factor of 10. If $A_0 = \infty$ and $R_1 C_1 = 10 \text{ ns}$, compute the frequency of the sinusoid.
21. The integrator of Fig. 8.52 must provide a pole at no higher than 1 Hz. If the values of $R_1$ and $C_1$ are limited to 10 kΩ and 1 nF, respectively, determine the required gain of the op amp.

22. Consider the integrator shown in Fig. 8.52 and suppose the op amp is modeled as shown in Fig. 8.44. Determine the transfer function $V_{out}/V_{in}$ and compare the location of the pole with that given by Eq. (8.37).

23. The op amp used in the integrator of Fig. 8.52 exhibits a finite output impedance and is modeled as depicted in Fig. 8.45. Compute the transfer function $V_{out}/V_{in}$ and compare the location of the pole with that given by Eq. (8.58).

24. The differentiator of Fig. 8.53 is used to amplify a sinusoidal input at a frequency of 1 MHz by a factor of 5. If $A_0 = \infty$, determine the value of $R_1C_1$.

25. We wish to design the differentiator of Fig. 8.53 for a pole frequency of 100 MHz. If the values of $R_1$ and $C_1$ cannot be lower than 1 kΩ and 10 pF, respectively, compute the required gain of the op amp.

26. Suppose the op amp in Fig. 8.53 exhibits a finite input impedance and is modeled as shown in Fig. 8.44. Determine the transfer function $V_{out}/V_{in}$ and compare the result with Eq. (8.42).
27. The op amp used in the differentiator of Fig. 8.53 suffers from a finite output impedance and is modeled as depicted in Fig. 8.45. Compute the transfer function and compare the result with Eq. (8.42).

28. Calculate the transfer function of the circuit shown in Fig. 8.54 if $A_0 = \infty$. What choice of component values reduces $|V_{out}/V_{in}|$ to unity?

29. Repeat Problem 28 if $A_0 < \infty$. Can the resistors and capacitors be chosen so as to reduce $|V_{out}/V_{in}|$ to unity?

30. Consider the voltage adder shown in Fig. 8.55. Plot $V_{out}$ as a function of time if $V_1 = V_0 \sin \omega t$ and $V_2 = V_0 \sin(3\omega t)$. Assume $R_1 = R_2$ and $A_0 = \infty$.

31. The op amp in Fig. 8.55 suffers from a finite gain. Calculate $V_{out}$ in terms of $V_1$ and $V_2$.

32. Due to a manufacturing error, a parasitic resistance $R_P$ has appeared in the adder of Fig. 8.56. Calculate $V_{out}$ in terms of $V_1$ and $V_2$ for $A_0 = \infty$ and $A_0 < \infty$. (Note that $R_P$ can also represent the input impedance of the op amp.)

33. The voltage adder of Fig. 8.55 employs an op amp having a finite output impedance, $R_{out}$. Using the op amp model depicted in Fig. 8.45, compute $V_{out}$ in terms of $V_1$ and $V_2$. 
34. Consider the voltage adder illustrated in Fig. 8.57, where $R_P$ is a parasitic resistance and the op amp exhibits a finite input impedance. With the aid of the op amp model shown in Fig. 8.44, determine $V_{out}$ in terms of $V_1$ and $V_2$.

35. Plot the current flowing through $D_1$ in the precision rectifier of Fig. 8.23(b) as a function of time for a sinusoidal input.

36. Plot the current flowing through $D_1$ in the precision rectifier of Fig. 8.24(a) as a function of time for a sinusoidal input.

37. Figure 8.58 shows a precision rectifier producing negative cycles. Plot $V_Y$, $V_{out}$, and the current flowing through $D_1$ as a function of time for a sinusoidal input.
38. Consider the precision rectifier depicted in Fig. 8.59, where a parasitic resistor $R_P$ has appeared in parallel with $D_1$. Plot $V_X$ and $V_Y$ as a function of time in response to a sinusoidal input. Use a constant-voltage model for the diode.

![Figure 8.59.](image)

39. Suppose $V_{in}$ in Fig. 8.25 varies from $-1$ V to $+1$ V. Sketch $V_{out}$ and $V_X$ as a function of $V_{in}$ if the op amp is ideal.

40. A student attempts to construct a noninverting logarithmic amplifier as illustrated in Fig. 8.60. Describe the operation of this circuit.

![Figure 8.60.](image)

41. Determine the small-signal voltage gain of the logarithmic amplifier depicted in Fig. 8.25 by differentiating both sides of (8.66) with respect to $V_{in}$. Plot the magnitude of the gain as a function of $V_{in}$ and explain why the circuit is said to provide a “compressive” characteristic.

42. The logarithmic amplifier of Fig. 8.25 must “map” an input range of 1 V to 10 V to an output range of $-1$ V to $-0.5$ V.

   (a) Determine the required values of $I_S$ and $R_1$.

   (b) Calculate the small-signal voltage gain at the two ends of the range.
43. The circuit illustrated in Fig. 8.61 can be considered a “true” square-root amplifier. Determine $V_{\text{out}}$ in terms of $V_{\text{in}}$ and compute the small-signal gain by differentiating the result with respect to $V_{\text{in}}$.

44. Calculate $V_{\text{out}}$ in terms of $V_{\text{in}}$ for the circuit shown in Fig. 8.62.

45. In the noninverting amplifier of Fig. 8.63, the op amp offset is represented by a voltage source in series with the inverting input. Calculate $V_{\text{out}}$.

46. Suppose each op amp in Fig. 8.29 suffers from an input offset of 3 mV. Determine the maximum offset error in $V_{\text{out}}$ if each amplifier is designed for a gain of 10.
47. For the inverting amplifier illustrated in Fig. 8.64, calculate $V_{\text{out}}$ if the op amp exhibits an input offset of $V_{\text{os}}$. Assume $A_0 = \infty$.

48. The integrator of Fig. 8.30(c) must operate with frequencies as low as 1 kHz while providing an output offset of less than 20 mV with an op amp offset of 3 mV. Determine the required values of $R_1$ and $R_2$ if $C_1 \leq 100$ pF.

49. Explain why dc offsets are not considered a serious issue in differentiators.

50. Explain the effect of op amp offset on the output of a logarithmic amplifier.

51. Suppose the input bias currents in Fig. 8.32 incur a small offset, i.e., $I_B = I_B + \Delta I$. Calculate $V_{\text{out}}$.

52. Repeat Problem 51 for the circuit shown in Fig. 8.34. What is the maximum allowable value of $R_1|R_2$ if the output error due to this mismatch must remain below a certain value, $\Delta V$?

53. A noninverting amplifier must provide a bandwidth of 100 MHz with a nominal gain of 4. Determine which one of the following op amp specifications are adequate:
   (a) $A_0 = 1000$, $f_1 = 50$ Hz.
   (a) $A_0 = 500$, $f_1 = 1$ kHz.

54. An inverting amplifier incorporates an op amp whose frequency response is given by Eq. (8.84). Determine the transfer function of the closed-loop circuit and compute the bandwidth.

55. Figure 8.65 shows an integrator employing an op amp whose frequency response is given by

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_0}} \quad (8.114)$$

Determine the transfer function of the overall integrator. Simplify the result if $\omega_0 \gg 1/(R_1C_1)$.
56. A noninverting amplifier with a nominal gain of 4 senses a sinusoid having a peak amplitude of 0.5 V. If the op amp provides a slew rate of 1 V/ns, what is the highest input frequency for which no slewing occurs?

57. The unity-gain buffer of Fig. 8.4 must be designed to drive a 100 Ω load with a gain error of 0.5%. Determine the required op amp gain if the op amp has an output resistance of 1 kΩ.

**Design Problems**

58. Design a noninverting amplifier with a nominal gain of 4, a gain error of 0.2%, and a total resistance of 20 kΩ. Assume the op amp has a finite gain but is otherwise ideal.

59. Design the inverting amplifier of Fig. 8.8(a) for a nominal gain of 8 and a gain error of 0.1%. Assume $R_{out} = 100$ Ω.

60. Design an integrator that attenuates input frequencies above 100 kHz and exhibits a pole at 100 Hz. Assume the largest available capacitor is 50 pF.

61. With a finite op amp gain, the step response of an integrator is a slow exponential rather than an ideal ramp. Design an integrator whose step response approximates $V(t) = \alpha t$ with an error less than 0.1% for the range $0 < V(t) < V_0$ (Fig. 8.66). Assume $\alpha = 10$ V/µs, $V_0 = 1$ V, and the capacitor must remain below 20 pF.

62. A voltage adder must realize the following function: $V_{out} = \alpha_1 V_1 + \alpha_2 V_2$, where $\alpha_1 = 0.5$ and $\alpha_2 = 1.5$. Design the circuit if the worst-case error in $\alpha_1$ or $\alpha_2$ must remain below 0.5% and the input impedance seen by $V_1$ or $V_2$ must exceed 10 kΩ.

63. Design a logarithmic amplifier that “compresses” an input range of $[0.1 \text{ V} \quad 2 \text{ V}]$ to an output range of $[-0.5 \text{ V} \quad 1 \text{ V}]$.

64. Design a logarithmic amplifier having a small-signal gain ($dV_{out} / dV_{in}$) of 2 at $V_{in} = 1$ V and 0.2 at $V_{in} = 2$ V. Assume the gain of the op amp is sufficiently high.
Figure 8.66.