1. An antenna can be modeled as a Thevenin equivalent having a sinusoidal voltage source \( V_0 \cos \omega t \) and an output resistance \( R_{\text{out}} \). Determine the average power delivered to a load resistance \( R_L \) and plot the result as a function of \( R_L \).

2. Determine the small-signal input resistance of the circuits shown in Fig. 5.105. Assume all diodes are forward-biased. (Recall from Chapter 3 that each diode behaves as a linear resistance if the voltage and current changes are small.)

3. Compute the input resistance of the circuits depicted in Fig. 5.106. Assume \( V_A = \infty \).

4. Compute the output resistance of the circuits depicted in Fig. 5.107.

5. Determine the input impedance of the circuits depicted in Fig. 5.108. Assume \( V_A = \infty \).

6. Compute the output impedance of the circuits shown in Fig. 5.109.

7. Compute the bias point of the circuits depicted in Fig. 5.110. Assume \( \beta = 100, I_S = 6 \times 10^{-16} \) A, and \( V_A = \infty \).
8. Construct the small-signal equivalent of each of the circuits in Problem 7.

9. Calculate the bias point of the circuits shown in Fig. 5.111. Assume $\beta = 100$, $I_S = 5 \times 10^{-16}$ A, and $V_A = \infty$.

10. Construct the small-signal equivalent of each of the circuits in Problem 9.
11. Consider the circuit shown in Fig. 5.112, where $\beta = 100$, $I_S = 6 \times 10^{-16}$ A, and $V_A = \infty$.

(a) What is the minimum value of $R_B$ that guarantees operation in the active mode?

(b) With the value found in $R_B$, how much base-collector forward bias is sustained if $\beta$ rises to 200?

12. In the circuit of Fig. 5.113, $\beta = 100$ and $V_A = \infty$.

(a) If the collector current of $Q_1$ is equal to 0.5 mA, calculate the value of $I_S$.

(b) If $Q_1$ is biased at the edge of saturation, calculate the value of $I_S$. 
13. The circuit of Fig. 5.114 must be designed for an input impedance of greater than 10 kΩ and a $g_m$ of at least $1/(260 \, \Omega)$. If $\beta = 100$, $I_s = 2 \times 10^{-17} \, \text{A}$, and $V_A = \infty$, determine the minimum allowable values of $R_1$ and $R_2$.

14. Repeat Problem 13 for a $g_m$ of at least $1/(26 \, \Omega)$. Explain why no solution exists.

15. We wish to design the stage depicted in Fig. 5.115 for a gain ($= g_m R_C$) of $A_0$ with an output impedance of $R_0$. What is the maximum achievable input impedance here? Assume $V_A = \infty$. 

Figure 5.113.

Figure 5.114.

Figure 5.115.
16. The circuit of Fig. 5.116 is designed for a collector current of 0.25 mA. Assume \( I_S = 6 \times 10^{-16} \) A, \( \beta = 100 \), and \( V_A = \infty \).

   (a) Determine the required value of \( R_1 \).

   (b) What is the error in \( I_C \) if \( R_E \) deviates from its nominal value by 5%?

17. In the circuit of Fig. 5.117, determine the maximum value of \( R_2 \) that guarantees operation of \( Q_1 \) in the active mode. Assume \( \beta = 100 \), \( I_S = 10^{-17} \) A, and \( V_A = \infty \).

18. Consider the circuit shown in Fig. 5.118, where \( I_{S1} = 2I_{S2} = 5 \times 10^{-16} \) A, \( \beta_1 = \beta_2 = 100 \), and \( V_A = \infty \).

   (a) Determine the collector currents of \( Q_1 \) and \( Q_2 \).

   (b) Construct the small-signal equivalent circuit.

19. In the circuit depicted in Fig. 5.119, \( I_{S1} = I_{S2} = 4 \times 10^{-16} \) A, \( \beta_1 = \beta_2 = 100 \), and \( V_A = \infty \).

   (a) Determine the operating point of the transistor.

   (b) Draw the small-signal equivalent circuit.
20. The circuit of Fig. 5.120 must be biased with a collector current of 2 mA. Compute the required value of $R_B$ if $I_S = 3 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

21. In the circuit of Fig. 5.121, $V_X = 1.1$ V. If $\beta = 100$, what is the value of $I_S$?

22. Consider the circuit shown in Fig. 5.122, where $I_S = 6 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$. Calculate the operating point of $Q_1$.

23. Due to a manufacturing error, a parasitic resistor, $R_P$, has appeared in series with the collector of $Q_1$ in Fig. 5.123. What is the minimum allowable value of $R_B$ if the base-collector forward bias must not exceed 200 mV? Assume $I_S = 3 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$. 
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24. In the circuit of Fig. 5.124, $I_S = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

   (a) Determine the operating point of $Q_1$.

   (b) Draw the small-signal equivalent circuit.

25. In the circuit of Fig. 5.125, $I_{S1} = I_{S2} = 3 \times 10^{-16}$ A and $V_A = \infty$.

   (a) Calculate $V_B$ such that $Q_1$ carries a collector current of 1 mA.

   (b) Construct the small-signal equivalent circuit.

26. Determine the bias point of each circuit shown in Fig. 5.126. Assume $\beta_{n_{PN}} = 2\beta_{p_{NP}} = 100$, 

Figure 5.121.

Figure 5.122.

Figure 5.123.
$I_S = 9 \times 10^{-16}$ A, and $V_A = \infty$.

27. Construct the small-signal model of the circuits in Problem 26.

28. Calculate the bias point of the circuits shown in Fig. 5.127. Assume $\beta_{n_{e-n}} = 2\beta_{p_{p-n}} = 100$, $I_S = 9 \times 10^{-16}$ A, and $V_A = \infty$.

29. Draw the small-signal model of the circuits in Problem 28.

30. We have chosen $R_B$ in Fig. 5.128 to place $Q_1$ at the edge of saturation. But the actual
value of this resistor can vary by $\pm 5\%$. Determine the forward- or reverse-bias across the base-collector junction at these two extremes. Assume $\beta = 50$, $I_S = 8 \times 10^{-16}$ A, and $V_A = \infty$.

31. Calculate the value of $R_E$ in Fig. 5.129 such that $Q_1$ sustains a reverse bias of 300 mV across its base-collector junction. Assume $\beta = 50$, $I_S = 8 \times 10^{-16}$ A, and $V_A = \infty$. What happens if the value of $R_E$ is halved?

32. If $\beta = 80$ and $V_A = \infty$, what value of $I_S$ yields a collector current of 1 mA in Fig. 5.130?
33. The topology depicted in Fig. 5.131(a) is called a "$V_{BE}$ multiplier." (The $n p n$ counterpart has a similar topology.) Constructing the circuit shown in Fig. 5.131(b), determine the collector-emitter voltage of $Q_1$ if the base current is negligible. (The $n p n$ counterpart can also be used.)

34. We wish to design the CE stage of Fig. 5.132 for a voltage gain of 20. What is the minimum allowable supply voltage if $Q_1$ must remain in the active mode? Assume $V_A = \infty$. 
35. The circuit of Fig. 5.133 must be designed for maximum voltage gain while maintaining $Q_1$ in the active mode. If $V_A = 10 \text{ V}$, calculate the required bias current.

$$I_C = I_S \exp \left( \frac{V_{BE}}{2V_T} \right), \quad (5.370)$$

and no Early effect. Compute the voltage gain for a bias current of 1 mA.
38. Determine the voltage gain and I/O impedances of the circuits shown in Fig. 5.136. Assume 
\( V_A = \infty \). Transistor \( Q_2 \) in Figs. 5.136(d) and (e) operates in soft saturation.

\[ V_{\text{in}} - V_{\text{out}} = V_{\text{CC}} \]

\[ Q_1 \]

\[ R_1 \]

\[ R_C \]

\[ \text{Figure 5.136.} \]

39. Repeat Problem 38 with \( V_A < \infty \).

40. Express the voltage gain of the stage depicted in Fig. 5.137 in terms of the collector bias 
\( I_C \), and \( V_T \). What is the gain if the dc voltage drops across \( R_C \) and \( R_E \) are equal to 
\( 20V_T \) and \( 5V_T \), respectively?

\[ V_{\text{in}} - V_{\text{out}} = V_{\text{CC}} \]

\[ R_C \]

\[ R_E \]

\[ Q_1 \]

\[ \text{Figure 5.137.} \]

41. We wish to design the degenerated stage of Fig. 5.138 for a voltage gain of 10 with \( Q_1 \)
operating at the edge of saturation. Calculate the bias current and the value of $R_C$ if $V_A = \infty$. Calculate the input impedance of the circuit.

42. Repeat Problem 41 for a voltage gain of 100. Explain why no solution exists. What is the maximum gain that can be achieved in this stage?

43. Determine the voltage gain and I/O impedances of the circuits shown in Fig. 5.139. Assume $V_A = \infty$.

44. Compute the voltage gain the I/O impedances of the circuits depicted in Fig. 5.140. Assume $V_A = \infty$. 

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Figure 5.138.

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Figure 5.139.

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Figure 5.140.
45. Calculate the output impedance of the circuits shown in Fig. 5.141. Assume $\beta \gg 1$.

46. Compare the output impedances of the circuits illustrated in Fig. 5.142. Assume $\beta \gg 1$.

47. Calculate $v_{out}/v_{in}$ for each of the circuits depicted in Fig. 5.143. Assume $I_s = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$. Also, assume the capacitors are very large.
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Figure 5.143.

48. The common-base stage of Fig. 5.144 is biased with a collector current of 2 mA. Assume $V_A = \infty$.

(a) Calculate the voltage gain and I/O impedances of the circuit.

(b) How should $V_B$ and $R_C$ be chosen to maximize the voltage gain with a bias current of 2 mA?

49. Determine the voltage gain of the circuits shown in Fig. 5.145. Assume $V_A = \infty$.

50. Compute the input impedance of the stages depicted in Fig. 5.146. Assume $V_A = \infty$.

51. Calculate the voltage gain and I/O impedances of the CB stage shown in Fig. 5.147. Assume $V_A < \infty$.

52. Consider the CB stage depicted in Fig. 5.148, where $\beta = 100$, $I_S = 8 \times 10^{-16}$ A, $V_A = \infty$, and $C_B$ is very large.

(a) Determine the operating point of $Q_1$. 
(b) Calculate the voltage gain and I/O impedances of the circuit.

53. Repeat Problem 52 for $C_B = 0$.

54. Compute the voltage gain and I/O impedances of the stage shown in Fig. 5.149 if $V_A = \infty$ and $C_B$ is very large.

55. Calculate the voltage gain and the I/O impedances of the stage depicted in Fig. 5.150 if $V_A = \infty$.

56. Calculate the voltage gain of the circuit shown in Fig. 5.151 if $V_A < \infty$. 
57. The circuit of Fig. 5.152 provides two outputs. If \( I_{S1} = 2I_{S2} \), determine the relationship between \( v_{out1}/v_{in} \) and \( v_{out2}/v_{in} \). Assume \( V_A = \infty \).
58. For $R_E = 100$ Ω in Fig. 5.153, determine the bias current of $Q_1$ such that the gain is equal to 0.8. Assume $V_A = \infty$.

59. The circuit of Fig. 5.153 must provide an input impedance of greater than 10 kΩ with a minimum gain of 0.9. Calculate the required bias current and $R_E$. Assume $\beta = 100$ and $V_A = \infty$.

60. A microphone having an output impedance $R_S = 200$ Ω drives an emitter follower as shown in Fig. 5.154. Determine the bias current such that the output impedance does not exceed 5 Ω. Assume $\beta = 100$ and $V_A = \infty$. 
61. Compute the voltage gain and I/O impedances of the circuits shown in Fig. 5.155. Assume $V_A = \infty$.

62. Figure 5.156 depicts a “Darlington pair,” where $Q_1$ plays a role somewhat similar to an emitter follower driving $Q_2$. Assume $V_A = \infty$. Note that $I_{C1} = I_{B2} = I_{C2}/\beta$. 
(a) If the emitter of $Q_2$ is grounded, determine the impedance seen at the base of $Q_1$.

(b) If the base of $Q_1$ is grounded, calculate the impedance seen at the emitter of $Q_2$.

(c) Compute the current gain of the pair, defined as $(I_{C1} + I_{C2})/I_{B1}$.

63. In the circuit shown in Fig. 5.157, $Q_2$ serves as a current source for the follower $Q_1$.

(a) Calculate the output impedance of the current source, $R_{CS}$.

(b) Replace $Q_2$ and $R_E$ with the impedance obtained in (a) and compute the voltage gain and I/O impedances of the circuit.

64. Determine the voltage gain of the follower depicted in Fig. 5.158. Assume $I_S = 7 \times 10^{-16}$ A, $\beta = 100$, and $V_A = 5$ V.

65. Figure 5.159 illustrates a cascade of an emitter follower and a common-emitter stage. Assume $V_A < \infty$.

(a) Calculate the input and output impedances of the circuit.

(b) Determine the voltage gain, $v_{out}/v_{in} = (v_x/v_{in})(v_{out}/v_x)$. 
66. Figure 5.160 shows a cascade of an emitter follower and a common-base stage. Assume $V_A = \infty$.

(a) Calculate the I/O impedances of the circuit.

(b) Calculate the voltage gain, $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$.

Design Problems

In the following problems, unless otherwise stated, assume $\beta = 100$, $I_S = 6 \times 10^{-16}$ A, and $V_A = \infty$.

67. Design the CE stage shown in Fig. 5.161 for a voltage gain of 10, and input impedance of greater than 5 kΩ, and an output impedance of 1 kΩ. If the lowest signal frequency of interest is 200 Hz, estimate the minimum allowable value of $C_B$.

68. We wish to design the CE stage of Fig. 5.162 for maximum voltage gain but with an output impedance no greater than 500 Ω. Allowing the transistor to experience at most 400 mV of base-collector forward bias, design the stage.

69. The stage depicted in Fig. 5.162 must achieve maximum input impedance but with a voltage gain of at least 20 and an output impedance of 1 kΩ. Design the stage.
70. The CE stage of Fig. 5.162 must be designed for minimum supply voltage but with a voltage gain of 15 and an output impedance of 2 kΩ. If the transistor is allowed to sustain a base-collector forward bias of 400 mV, design the stage and calculate the required supply voltage.

71. We wish to design the CE stage of Fig. 5.162 for minimum power dissipation. If the voltage gain must be equal to $A_0$, determine the trade-off between the power dissipation and the output impedance of the circuit.

72. Design the CE stage of Fig. 5.162 for a power budget of 1 mW and a voltage gain of 20.

73. Design the degenerated CE stage of Fig. 5.163 for a voltage gain of 10 and an output impedance of 500 Ω. Assume $R_E$ sustains a voltage drop of 300 mV and the current flowing through $R_1$ is approximately the base current.

74. The stage of Fig. 5.163 must be designed for maximum voltage gain but an output impedance of no greater than 1 kΩ. Design the circuit, assuming that $R_E$ sustains 200 mV, and the current flowing through $R_1$ is approximately 10 times the base current, and $Q_1$ experiences a maximum base-collector forward bias of 400 mV.
75. Design the stage of Fig. 5.163 for a power budget of 5 mW, a voltage gain of 5, and a voltage drop of 200 mV across $R_E$. Assume the current flowing through $R_1$ is approximately 10 times the base current.

76. Design the common-base stage shown in Fig. 5.164 for a voltage gain of 20 and an input impedance of 50 $\Omega$. Assume a voltage drop of $10V_T = 260$ mV across $R_E$ so that this resistor does not affect the input impedance significantly. Also, assume the current flowing through $R_1$ is approximately 10 times the base current, and the lowest frequency of interest is 200 Hz.

77. The CB amplifier of Fig. 5.164 must achieve a voltage gain of 8 with an output impedance of 500 $\Omega$. Design the circuit with the same assumptions as those in Problem 76.

78. We wish to design the CB stage of Fig. 5.164 for an output impedance of 200 $\Omega$ and a voltage gain of 20. What is the minimum required power dissipation?

79. Design the CB amplifier of Fig. 5.164 for a power budget of 5 mW and a voltage gain of 10. Make the same assumptions as those in Problem 76.
80. Design the CB stage of Fig. 5.164 for the minimum supply voltage if an input impedance of 50 Ω and a voltage gain of 20 are required. Make the same assumptions as those in Problem 76.

81. Design the emitter follower shown in Fig. 5.165 for a voltage gain of 0.85 and an input impedance of greater than 10 kΩ. Assume $R_L = 200 \, \Omega$.

82. The follower of Fig. 5.165 must consume 5 mW of power while achieving a voltage gain of 0.9. What is the minimum load resistance, $R_L$, that it can drive? What is the required value of $R_L$?

83. The follower shown in Fig. 5.166 must drive a load resistance, $R_L = 50 \, \Omega$, with a voltage gain of 0.8. Design the circuit assuming that the lowest frequency of interest is 100 MHz. (Hint: select the voltage drop across $R_E$ to be much greater than $V_T$ so that this resistor does not affect the voltage gain significantly.)